

# Keysight N6469A eDP Test Application

# Notices

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## Safety Notices

### CAUTION

A **CAUTION** notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in damage to the product or loss of important data. Do not proceed beyond a **CAUTION** notice until the indicated conditions are fully understood and met.

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### WARNING

A **WARNING** notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in personal injury or death. Do not proceed beyond a **WARNING** notice until the indicated conditions are fully understood and met.

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## In This Book

This book is your guide to programming the Keysight Technologies N6469A eDP Test Application.

- **Chapter 1**, “Introduction to Programming,” starting on page 7, describes compliance application programming basics.
- **Chapter 2**, “Configuration Variables and Values,” starting on page 9, **Chapter 3**, “Test Names and IDs,” starting on page 39, and **Chapter 4**, “Instruments,” starting on page 75, provide information specific to programming the N6469A eDP Test Application.

### How to Use This Book

Programmers who are new to compliance application programming should read all of the chapters in order. Programmers who are already familiar with this may review chapters 2, 3, and 4 for changes.



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# 1 Introduction to Programming

Remote Programming Toolkit / 8

This chapter introduces the basics for remote programming a compliance application. The programming commands provide the means of remote control. Basic operations that you can do remotely with a computer and a compliance app running on an oscilloscope include:

- Launching and closing the application.
- Configuring the options.
- Running tests.
- Getting results.
- Controlling when and where dialogs get displayed
- Saving and loading projects.

You can accomplish other tasks by combining these functions.

## Remote Programming Toolkit

The majority of remote interface features are common across all the Keysight Technologies, Inc. family of compliance applications. Information on those features is provided in the N5452A Compliance Application Remote Programming Toolkit available for download from Keysight here: [www.keysight.com/find/rpi](http://www.keysight.com/find/rpi). The N6469A eDP Test Application uses Remote Interface Revision 3.40. The help files provided with the toolkit indicate which features are supported in this version.

In the toolkit, various documents refer to "application-specific configuration variables, test information, and instrument information". These are provided in Chapters 2, 3, and 4 of this document, and are also available directly from the application's user interface when the remote interface is enabled (View>Preferences::Remote tab::Show remote interface hints). See the toolkit for more information.



## 2 Configuration Variables and Values

The following table contains a description of each of the N6469A eDP Test Application options that you may query or set remotely using the appropriate remote interface method. The columns contain this information:

- GUI Location – Describes which graphical user interface tab contains the control used to change the value.
- Label – Describes which graphical user interface control is used to change the value.
- Variable – The name to use with the SetConfig method.
- Values – The values to use with the SetConfig method.
- Description – The purpose or function of the variable.

For example, if the graphical user interface contains this control on the **Set Up** tab:

- Enable Advanced Features

then you would expect to see something like this in the table below:

**Table 1** Example Configuration Variables and Values

GUI Location	Label	Variable	Values	Description
Set Up	Enable Advanced Features	EnableAdvanced	True, False	Enables a set of optional features.

and you would set the variable remotely using:

```
ARSL syntax  
-----  
arsl -a ipaddress -c "SetConfig 'EnableAdvanced' 'True'"
```

```
C# syntax
-----
remoteAte.SetConfig("EnableAdvanced", "True");
```

Here are the actual configuration variables and values used by this application:

**NOTE**

Some of the values presented in the table below may not be available in certain configurations. Always perform a "test run" of your remote script using the application's graphical user interface to ensure the combinations of values in your program are valid.

**NOTE**

The file, "ConfigInfo.txt", which may be found in the same directory as this help file, contains all of the information found in the table below in a format suitable for parsing.

**Table 2** Configuration Variables and Values

GUI Location	Label	Variable	Values	Description
Configure	AC Common Mode Noise Edges	ACCommonModeNoiseEdge	(Accepts user-defined text), 100, 1000, 10000, 100000, 200000	Set the number of edges measured for the AC Common Mode Noise Test.
Configure	AC Common Mode Noise Filter	ACCommonModeNoiseFilter	None, HighPassFilter, LowPassFilter	Select the type of filter used in AC Common Mode Noise Test.
Configure	AC Common Mode Noise Filter Cutoff Frequency	ACCommonModeNoiseFilterCutoffFrequency	(Accepts user-defined text), 50MHz, 500MHz, 1000MHz	Set the 3 dB cutoff frequency of the filter used in AC Common Mode Noise Test. This configuration only applicable when the [AC Common Mode Noise Filter] config variable is set to [High Pass Filter] or [Low Pass Filter]. Please specify the value in following format: "XMHz", "XkHz" or "XHz", where X is an integer.
Configure	AC Common Mode Noise Memory Depth (kpts)	ACCommonModeNoiseMemoryDepth	(Accepts user-defined text), 2000, 5000, 8000	Set the memory depth for each acquisition in AC Common Mode Noise Test. Unit: kpts.
Configure	AUX Clock Recovery Filter	AUXClockRecoveryFilter	true, false	Define if clock is recovered after applying a low pass filter.
Configure	AUX Decode Filter	AUXDecodeFilter	true, false	Define whether to apply filter before decoding traffic for AUX sensitivity tests.
Configure	AUX Eye Acquisition	AUXEyeAcquisition	(Accepts user-defined text), 1, 10, 5	Specify number of acquisitions needed for AUX test measurement
Configure	AUX Eye Mask Center	AUXEyeMaskCenter	0 V, AutoOffset	Define the vertical mask center position of eye mask.

**Table 2** Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	AUX Eye Mask Width Reference	AUXEyeMaskWidthReference	Nominal, Average	Define the width of Mask width reference either based on nominal rate or measured data rate.
Configure	AUX Memory Depth	AUXMemDepth	(Accepts user-defined text), 200000, 500000, 1000000, 2000000, 4000000	Specify the memory depth used for AUX test measurement. Note: 80k scope only supports up to 2M points only.
Configure	AUX Min Failure Required	AUXMaxFailAcquisition	(Accepts user-defined text), 10, 100, 1000	When failure in AUX sensitivity is detected, you might stop the AUX traffic decoding immediately to save test time. This configuration allows you to set the minimum number of acquisitions to analyze before exit test.
Configure	AUX Probe Check	AUXProbeCheck	Enable, Disable	Enable or disable probe check while running AUXtests.
Configure	AUX Sampling Rate, GSa/s	AUXSamplingRate	(Accepts user-defined text), 1, 5, 10, 20, 40	Specify the sampling rate used for AUX test measurement
Configure	AUX Sensitivity Calibration Acquisition	AUXSensitivityCalibrationAcquisition	(Accepts user-defined text), 1, 3, 5, 10	Define the number of acquisition to measure for AUX sensitivity Calibration.
Configure	AUX Sensitivity Maximum VSwing (V)	AUXSensitivityMaxVSwing	(Accepts user-defined text), 0.28, 0.26	Define the maximum Vswing limit for AUX Sensitivity tests.
Configure	AUX Sensitivity Memory Depth	AUXSensitivityMemDepth	(Accepts user-defined text), 2000000, 5000000, 10000000, 20000000	Specify the memory depth used for AUX Sensitivity test.
Configure	AUX Sensitivity Minimum VSwing (V)	AUXSensitivityMinVSwing	(Accepts user-defined text), 0.28, 0.24	Define the minimum Vswing limit for AUX Sensitivity tests.
Configure	AUX Sensitivity Sampling Rate, MSa/s	AUXSensitivitySamplingRate	(Accepts user-defined text), 5, 10	Specify the sampling rate used for AUX Sensitivity test in MSa/s
Configure	AUX Sensitivity Test Level(mV)	AUXSensitivityTestLevel	(Accepts user-defined text), 240, 260, 270, 270	Define the number of acquisition to measure for AUX sensitivity Calibration.
Configure	AUX Sensitivity Test Method	AUXSensitivityTestMethod	Scope Method, Reference Device Method	Define method to test AUX sensitivity either through Scope Decoding or with built in test from Reference device. If Reference Device does not have built in test, then Scope Decoding method is used.

**Table 2** Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	AUX Traffic Decode Count	AUXTrafficDecodeCount	(Accepts user-defined text), 10, 100, 20, 1000	Set the total amount of traffic required before the test completes.
Configure	Band width Reduction	BWReduction	AUTO, 4.0E9, 6.0E9, 8.0E9, 13.0E9, 20.0E9, 32.0E9, MAX	Set the band width for the acquisition setup of the oscilloscope. This configuration only applicable when the Enhance Band width or Noise Reduction option is installed on the oscilloscope.
Configure	Cable Embedding	CableEmbedding	True, False	Enable or disable cable embedding for TP3_EQ tests.
Configure	Channel Skew	ChannelSkew	Disable, Enable	Select to enable or disable channel skew. For [Disable], the skew of all the channels will be default to 0 before each run of the test.
Configure	Clock Recovery Damping Factor - HBR (Second Order PLL Only)	CDR_DampingFactor_HBR	(Accepts user-defined text), 1.43, 1.51, 1.6, N/A	Set the damping factor used by the second order PLL to recover the clock for HBR. This configuration only applicable when the [Clock Recovery Order] config variable is set to second order PLL clock recovery.
Configure	Clock Recovery Damping Factor - HBR2 (Second Order PLL Only)	CDR_DampingFactor_HBR2	(Accepts user-defined text), 1.0, 1.43, 1.51, 1.6, N/A	Set the damping factor used by the second order PLL to recover the clock for HBR2. This configuration only applicable when the [Clock Recovery Order] config variable is set to second order PLL clock recovery.
Configure	Clock Recovery Damping Factor - HBR3 (Second Order PLL Only)	CDR_DampingFactor_HBR3	(Accepts user-defined text), 1.0, 1.43, 1.51, 1.6, N/A	Set the damping factor used by the second order PLL to recover the clock for HBR3. This configuration only applicable when the [Clock Recovery Order] config variable is set to second order PLL clock recovery.
Configure	Clock Recovery Damping Factor - Link Rate 1 (Second Order PLL Only)	CDR_DampingFactor_LinkRate1	(Accepts user-defined text), 1.43, 1.51, 1.6, N/A	Set the damping factor used by the second order PLL to recover the clock for Link Rate 1. This configuration only applicable when the [Clock Recovery Order] config variable is set to second order PLL clock recovery.

**Table 2** Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Clock Recovery Damping Factor - Link Rate 2 (Second Order PLL Only)	CDR_DampingFactor_LinkRate 2	(Accepts user-defined text), 1.43, 1.51, 1.6, N/A	Set the damping factor used by the second order PLL to recover the clock for Link Rate 2. This configuration only applicable when the [Clock Recovery Order] config variable is set to second order PLL clock recovery.
Configure	Clock Recovery Damping Factor - Link Rate 3 (Second Order PLL Only)	CDR_DampingFactor_LinkRate 3	(Accepts user-defined text), 1.0, 1.43, 1.51, 1.6, N/A	Set the damping factor used by the second order PLL to recover the clock for Link Rate 3. This configuration only applicable when the [Clock Recovery Order] config variable is set to second order PLL clock recovery.
Configure	Clock Recovery Damping Factor - Link Rate 4 (Second Order PLL Only)	CDR_DampingFactor_LinkRate 4	(Accepts user-defined text), 1.0, 1.43, 1.51, 1.6, N/A	Set the damping factor used by the second order PLL to recover the clock for Link Rate 4. This configuration only applicable when the [Clock Recovery Order] config variable is set to second order PLL clock recovery.
Configure	Clock Recovery Damping Factor - RBR (Second Order PLL Only)	CDR_DampingFactor_RBR	(Accepts user-defined text), 1.43, 1.51, 1.6, N/A	Set the damping factor used by the second order PLL to recover the clock for RBR. This configuration only applicable when the [Clock Recovery Order] config variable is set to second order PLL clock recovery.
Configure	Clock Recovery Damping Factor -RBR/HBR (Second Order Only)	DampingFactor	(Accepts user-defined text), 1.43, 1.51, 1.6, N/A	Set the damping factor that is used in designing the second order PLL to recover the clock.(apply when user select Second Order PLL Clock Recovery)
Configure	Clock Recovery Loop Band width - HBR	CDR_BW_HBR	(Accepts user-defined text), 20.0MHz, 10.0MHz	Set the 3 dB band width of the loop filter used by the PLL to recover the clock for HBR. This configuration only applicable when the [Clock Recovery Settings Mode] config variable is set to [Auto]. Please specify the value in following format: "XMHz", "XkHz" or "XHz", where X is an integer.

**Table 2** Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Clock Recovery Loop Bandwidth - HBR2	CDR_BW_HBR2	(Accepts user-defined text), 20.0MHz, 10.0MHz	Set the 3 dB bandwidth of the loop filter used by the PLL to recover the clock for HBR2. This configuration only applicable when the [Clock Recovery Settings Mode] config variable is set to [Auto]. Please specify the value in following format: "XMHz", "XkHz" or "XHz", where X is an integer.
Configure	Clock Recovery Loop Bandwidth - HBR3	CDR_BW_HBR3	(Accepts user-defined text), 20.0MHz, 10.0MHz	Set the 3 dB bandwidth of the loop filter used by the PLL to recover the clock for HBR3. This configuration only applicable when the [Clock Recovery Settings Mode] config variable is set to [Auto]. Please specify the value in following format: "XMHz", "XkHz" or "XHz", where X is an integer.
Configure	Clock Recovery Loop Bandwidth - Link Rate 1	CDR_BW_LinkRate1	(Accepts user-defined text), 10.8MHz, 5.4MHz	Set the 3 dB bandwidth of the loop filter used by the PLL to recover the clock for Link Rate 1. This configuration only applicable when the [Clock Recovery Settings Mode] config variable is set to [Manual]. Please specify the value in following format: "XMHz", "XkHz" or "XHz", where X is an integer.
Configure	Clock Recovery Loop Bandwidth - Link Rate 2	CDR_BW_LinkRate2	(Accepts user-defined text), 20.0MHz, 10.0MHz	Set the 3 dB bandwidth of the loop filter used by the PLL to recover the clock for Link Rate 2. This configuration only applicable when the [Clock Recovery Settings Mode] config variable is set to [Manual]. Please specify the value in following format: "XMHz", "XkHz" or "XHz", where X is an integer.
Configure	Clock Recovery Loop Bandwidth - Link Rate 3	CDR_BW_LinkRate3	(Accepts user-defined text), 20.0MHz, 10.0MHz	Set the 3 dB bandwidth of the loop filter used by the PLL to recover the clock for Link Rate 3. This configuration only applicable when the [Clock Recovery Settings Mode] config variable is set to [Manual]. Please specify the value in following format: "XMHz", "XkHz" or "XHz", where X is an integer.

**Table 2** Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Clock Recovery Loop Bandwidth - Link Rate 4	CDR_BW_LinkRate4	(Accepts user-defined text), 20.0MHz, 10.0MHz	Set the 3 dB bandwidth of the loop filter used by the PLL to recover the clock for Link Rate 4. This configuration only applicable when the [Clock Recovery Settings Mode] config variable is set to [Manual]. Please specify the value in following format: "XMHz", "XkHz" or "XHz", where X is an integer.
Configure	Clock Recovery Loop Bandwidth - RBR	CDR_BW_RBR	(Accepts user-defined text), 10.8MHz, 5.4MHz	Set the 3 dB bandwidth of the loop filter used by the PLL to recover the clock for RBR. This configuration only applicable when the [Clock Recovery Settings Mode] config variable is set to [Auto]. Please specify the value in following format: "XMHz", "XkHz" or "XHz", where X is an integer.
Configure	Clock Recovery Loop Bandwidth Correction Mode	CDR_BW_CorrectionMode	Enable, Disable	Enable or disable clock recovery loop bandwidth correction mode. This configuration only applicable when the [Clock Recovery Order] config variable is set to second order PLL clock recovery.
Configure	Clock Recovery Order	ClockRecoveryOrder	1st, 2nd	Set the order of PLL clock recovery to either first order PLL clock recovery method or second order PLL clock recovery method.
Configure	Clock Recovery Settings Mode	ClockRecoverySettingsMode	Auto, Manual	Set the mode for clock recovery setting to either [Auto] mode or [Manual] mode. For [Auto] mode, the clock recovery setting is selected based on the bit rate measured. For [Manual] mode, the clock recovery setting is selected based on the link rate.
Configure	Custom Transfer Function File Name	CustomTFFilename	(Accepts user-defined text), CustomEmbedded	Define the custom transfer function file name to be used for TP3_EQ test if [Use Custom Transfer Function] is "True". The transfer function file must be inside the ProgramFiles->Agilent->Infiniium->Apps->eDPTest->App->Config->TransferFunction->Custom folder.
Configure	De-Embed Delay	DeEmbedDelay	(Accepts user-defined text), True, False	Select to include or remove filter delay when de-embedding.

**Table 2** Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Equalizer Enable	EqualizerEnable	True, False	Select to enable or disable equalizer when performing tests at TP3_EQ test point. For [True], the equalizer will be enabled when performing tests at TP3_EQ test point. For [False], the equalizer will be disabled when performing tests at TP3_EQ test point.
Configure	Expert Mode	ExpertMode	Off, On	Select to enable or disable expert mode.
Configure	Eye Diagram Custom Eye Mask	EyeDiagramCustomEyeMask	False, True	Select to enable custom eye mask to be used in Eye Diagram Test.
Configure	Eye Diagram Eye Mask Height Location	EyeDiagramEyeMaskHeightLocation	Dynamic, Fixed	Select the location of eye height on the eye mask used in Eye Diagram Test.
Configure	Eye Diagram Eye Mask Movement	EyeDiagramEyeMaskMovement		Select the type of movement performed on the eye mask used in Eye Diagram Test. For [Fixed] mode, the mask will not be shifted and aligned. For [Find Pass] mode, the mask will automatically be shifted and aligned horizontally within +/-0.25UI until no violation occurs. For [Find Margin] mode, the mask will automatically be shifted and aligned horizontally within +/-0.25UI to search for maximum margin with no violation occurs.
Configure	Eye Diagram Eye Mask Scale	EyeDiagramEyeMaskScale	Absolute, Normalized	Select the type of scale performed on the eye mask used in Eye Diagram Test.
Configure	Eye Diagram Folding Bits	EyeDiagramFoldingBits	AUTO, BOTH, DEEmphasis, TRANSition	Select to folding bits used in Eye Diagram Test. For [Auto], [Both] folding bits will be used for Pre-Emphasis Level 0 and [Transition] folding bits will be used for other Pre-Emphasis Level.
Configure	Eye Diagram Include Random Noise	EyeDiagramIncludeRandomNoise	False, True	Select to include random noise on the eye mask used in Eye Diagram Test. This configuration is only applicable when the [Eye Diagram Eye Mask Height Location] config variable is set to [Dynamic].
Configure	Eye Diagram Memory Depth (kpts)	EyeDiagramMemoryDepth	(Accepts user-defined text), 2000, 5000, 8000	Set the memory depth for each acquisition in Eye Diagram Test. Unit: kpts.



**Table 2** Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Eye Diagram Passing End Location (UI)	EyeDiagramPassEndLocation	(Accepts user-defined text), 0.625	Set the end passing unit interval location for Eye Diagram Test. Unit: UI.
Configure	Eye Diagram Passing Start Location (UI)	EyeDiagramPassStartLocation	(Accepts user-defined text), 0.375	Set the start passing unit interval location for Eye Diagram Test. Unit: UI.
Configure	Eye Diagram UI Count	EyeDiagramUICount	10000, 100000, 1000000, 10000000, 100000000	Select the number of UI measured for Eye Diagram Test.
Configure	Fall Time Location (D10.2)	FallTimeLocationD10_2	(Accepts user-defined text), 1	Set the zero based pattern bit location used for D10.2 fall time measurement in Fall Time Test.
Configure	Fall Time Location (Other Pattern)	FallTimeLocationOtherPattern	(Accepts user-defined text), 1	Set the zero based pattern bit location used for Other Pattern fall time measurement in Fall Time Test.
Configure	Fall Time Location (PLTPAT)	FallTimeLocationPLTPAT	(Accepts user-defined text), 1	Set the zero based pattern bit location used for PLTPAT fall time measurement in Fall Time Test.
Configure	Fall Time Location (PRBS 7)	FallTimeLocationPRBS7	(Accepts user-defined text), 1	Set the zero based pattern bit location used for PRBS 7 fall time measurement in Fall Time Test.
Configure	Fall Time Location (PRBS 9)	FallTimeLocationPRBS9	(Accepts user-defined text), 1	Set the zero based pattern bit location used for PRBS 9 fall time measurement in Fall Time Test.
Configure	Fall Time Location (Random Pattern)	FallTimeLocationRandomPattern	(Accepts user-defined text), 1	Set the zero based pattern bit location used for Random Pattern fall time measurement in Fall Time Test.
Configure	Fall Time Pattern (D10.2)	FallTimePatternD10_2	(Accepts user-defined text), 10	Set the triggering pattern used for D10.2 fall time measurement in Fall Time Test.
Configure	Fall Time Pattern (Other Pattern)	FallTimePatternOtherPattern	(Accepts user-defined text), 10	Set the triggering pattern used for Other Pattern fall time measurement in Fall Time Test.
Configure	Fall Time Pattern (PLTPAT)	FallTimePatternPLTPAT	(Accepts user-defined text), 100000	Set the triggering pattern used for PLTPAT fall time measurement in Fall Time Test.
Configure	Fall Time Pattern (PRBS 7)	FallTimePatternPRBS7	(Accepts user-defined text), 10	Set the triggering pattern used for PRBS 7 fall time measurement in Fall Time Test.

**Table 2** Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Fall Time Pattern (PRBS 9)	FallTimePattern PRBS9	(Accepts user-defined text), 10	Set the triggering pattern used for PRBS 9 fall time measurement in Fall Time Test.
Configure	Fall Time Pattern (Random Pattern)	FallTimePattern RandomPattern	(Accepts user-defined text), 10	Set the triggering pattern used for Random Pattern fall time measurement in Fall Time Test.
Configure	Inter Pair Skew Edges	InterPairSkewE dge	(Accepts user-defined text), 100, 500, 1000	Set the number of edges measured for the Inter Pair Skew Test.
Configure	Inter Pair Skew Maximum Retries	InterPairSkew MaxRetries	20, 50, 100	Set the number of retries for the Inter Pair Skew Test.
Configure	Inter Pair Skew Memory Depth (kpts)	InterPairSkew MemoryDepth	(Accepts user-defined text), 2000, 5000, 8000	Set the memory depth for each acquisition in Inter Pair Skew Test. Unit: kpts.
Configure	Inter Pair Skew Middle Threshold Type	InterPairSkew MiddleThreshol dType	FixedVoltage, ThresholdMode	Select the type of middle threshold for the Inter Pair Skew Test.
Configure	Inter Pair Skew Middle Threshold Voltage (V)	InterPairSkew MiddleThreshol dVoltage	(Accepts user-defined text), 0	Set the middle threshold voltage for the Inter Pair Skew Test. Unit: Volt. This configuration only applicable when the [Inter Pair Skew Middle Threshold] config variable is set to [Fixed Voltage].
Configure	Inter Pair Skew Pattern (HBR2CPAT)	InterPairSkewP atternHBR2CP AT	(Accepts user-defined text), 0000001, 011111	Set the triggering pattern used for HBR2CPAT inter pair skew measurement in Inter Pair Skew Test.
Configure	Inter Pair Skew Pattern (Other Pattern)	InterPairSkewP atternOtherPatt ern	(Accepts user-defined text), 0000001, 0000111	Set the triggering pattern used for Other Pattern inter pair skew measurement in Inter Pair Skew Test.
Configure	Inter Pair Skew Pattern (PRBS 7)	InterPairSkewP atternPRBS7	(Accepts user-defined text), 0000001, 0000111	Set the triggering pattern used for PRBS 7 inter pair skew measurement in Inter Pair Skew Test.
Configure	Inter Pair Skew Pattern (PRBS 9)	InterPairSkewP atternPRBS9	(Accepts user-defined text), 0000001, 0000111	Set the triggering pattern used for PRBS 9 inter pair skew measurement in Inter Pair Skew Test.
Configure	Inter Pair Skew Pattern (Random Pattern)	InterPairSkewP atternRandomP attern	(Accepts user-defined text), 0000001, 0000111	Set the triggering pattern used for Random Pattern inter pair skew measurement in Inter Pair Skew Test.

**Table 2** Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Inter Pair Skew Pattern Match Bit Number	InterPairSkewPatternMatchBitNum	(Accepts user-defined text), 1, 10, 100, 200	Set the number of bit for pattern matching in Inter Pair Skew Test.
Configure	Intra Pair Skew Edges	IntraPairSkewEdge	(Accepts user-defined text), 100, 500, 1000	Set the number of edges measured for the Intra Pair Skew Test.
Configure	Intra Pair Skew Lane+ Fall Lane- Rise Location (D10.2)	IntraPairSkewFallRiseLocationD10_2	(Accepts user-defined text), 1	Set the zero based pattern bit location used for D10.2 Lane+ fall to Lane- rise skew measurement in Intra Pair Skew Test.
Configure	Intra Pair Skew Lane+ Fall Lane- Rise Location (HBR2CPAT)	IntraPairSkewFallRiseLocationHBR2CPAT	(Accepts user-defined text), 1	Set the zero based pattern bit location used for HBR2CPAT Lane+ fall to Lane- rise skew measurement in Intra Pair Skew Test.
Configure	Intra Pair Skew Lane+ Fall Lane- Rise Pattern (D10.2)	IntraPairSkewFallRisePatternD10_2	(Accepts user-defined text), 10	Set the triggering pattern used for D10.2 Lane+ fall to Lane- rise skew measurement in Intra Pair Skew Test.
Configure	Intra Pair Skew Lane+ Fall Lane- Rise Pattern (HBR2CPAT)	IntraPairSkewFallRisePatternHBR2CPAT	(Accepts user-defined text), 10	Set the triggering pattern used for HBR2CPAT Lane+ fall to Lane- rise skew measurement in Intra Pair Skew Test.
Configure	Intra Pair Skew Lane+ Rise Lane- Fall Location (D10.2)	IntraPairSkewRiseFallLocationD10_2	(Accepts user-defined text), 1	Set the zero based pattern bit location used for D10.2 Lane+ rise to Lane- fall skew measurement in Intra Pair Skew Test.
Configure	Intra Pair Skew Lane+ Rise Lane- Fall Location (HBR2CPAT)	IntraPairSkewRiseFallLocationHBR2CPAT	(Accepts user-defined text), 1	Set the zero based pattern bit location used for HBR2CPAT Lane+ rise to Lane- fall skew measurement in Intra Pair Skew Test.
Configure	Intra Pair Skew Lane+ Rise Lane- Fall Pattern (D10.2)	IntraPairSkewRiseFallPatternD10_2	(Accepts user-defined text), 01	Set the triggering pattern used for D10.2 Lane+ rise to Lane- fall skew measurement in Intra Pair Skew Test.

**Table 2** Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Intra Pair Skew Lane+ Rise Lane- Fall Pattern (HBR2CPAT)	IntraPairSkewRiseFallPatternHBR2CPAT	(Accepts user-defined text), 01	Set the triggering pattern used for HBR2CPAT Lane+ rise to Lane- fall skew measurement in Intra Pair Skew Test.
Configure	Intra Pair Skew Memory Depth (kpts)	IntraPairSkewMemoryDepth	(Accepts user-defined text), 100, 500, 1000	Set the memory depth for each acquisition in Intra Pair Skew Test. Unit: kpts.
Configure	Intra Pair Skew VH Location (D10.2)	IntraPairSkewVHLocationD10_2	(Accepts user-defined text), 1.6, 1.75	Set the pattern bit location used for D10.2 VH transition measurement in Intra Pair Skew Test. Use comma separated location value, such as [x,y]. Where x is the start location, y is the end location.
Configure	Intra Pair Skew VH Location (HBR2CPAT)	IntraPairSkewVHLocationHBR2CPAT	(Accepts user-defined text), 1.6, 1.75	Set the pattern bit location used for HBR2CPAT VH transition measurement in Intra Pair Skew Test. Use comma separated location value, such as [x,y]. Where x is the start location, y is the end location.
Configure	Intra Pair Skew VH Pattern (D10.2)	IntraPairSkewVHPatternD10_2	(Accepts user-defined text), 01	Set the triggering pattern used for D10.2 VH measurement in Intra Pair Skew Test.
Configure	Intra Pair Skew VH Pattern (HBR2CPAT)	IntraPairSkewVHPatternHBR2CPAT	(Accepts user-defined text), 01	Set the triggering pattern used for HBR2CPAT VH measurement in Intra Pair Skew Test.
Configure	Intra Pair Skew VL Location (D10.2)	IntraPairSkewVLLocationD10_2	(Accepts user-defined text), 1.6, 1.75	Set the pattern bit location used for D10.2 VL transition measurement in Intra Pair Skew Test. Use comma separated location value, such as [x,y]. Where x is the start location, y is the end location.
Configure	Intra Pair Skew VL Location (HBR2CPAT)	IntraPairSkewVLLocationHBR2CPAT	(Accepts user-defined text), 1.6, 1.75	Set the pattern bit location used for HBR2CPAT VL transition measurement in Intra Pair Skew Test. Use comma separated location value, such as [x,y]. Where x is the start location, y is the end location.
Configure	Intra Pair Skew VL Pattern (D10.2)	IntraPairSkewVLPatternD10_2	(Accepts user-defined text), 10	Set the triggering pattern used for D10.2 VL measurement in Intra Pair Skew Test.

**Table 2** Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Intra Pair Skew VL Pattern (HBR2CPAT)	IntraPairSkewVLPatternHBR2CPAT	(Accepts user-defined text), 10	Set the triggering pattern used for HBR2CPAT VL measurement in Intra Pair Skew Test.
Configure	Jitter Bit Error Rate	JitterBER	E9, E10, E11, E12, E13, E14	Select the bit error rate (BER) for the extrapolation of total jitter.
Configure	Jitter ISI Filter Lag	JitterISIFilterLag	(Accepts user-defined text), 5, 6	Select the ISI filter lag used for the jitter separation test. This configuration only applicable when the [Jitter Pattern Length] config variable is set to [Arbitrary].
Configure	Jitter ISI Filter Lead	JitterISIFilterLead	(Accepts user-defined text), -2, -3	Select the ISI filter lead used for the jitter separation test. This configuration only applicable when the [Jitter Pattern Length] config variable is set to [Arbitrary].
Configure	Jitter Memory Depth (kpts)	JitterMemoryDepth	(Accepts user-defined text), 2000, 5000, 8000	Set the memory depth for each acquisition in jitter separation test. Unit: kpts.
Configure	Jitter Pattern Length	JitterPatternLength	Arbitrary, Periodic	Select the pattern length used for the jitter separation test.
Configure	Jitter Separation Edges	JitterSeparationEdge	(Accepts user-defined text), 10000, 50000, 1000000	Set the number of edges measured for the jitter separation test.
Configure	Level Memory Depth (kpts)	LevelMemoryDepth	(Accepts user-defined text), 100, 500, 1000	Set the memory depth for each acquisition to be averaged and measured in Differential Voltage Level Test and Pre-Emphasis Level Test. Unit: kpts.
Configure	Level Pattern Count	LevelPatternCount	(Accepts user-defined text), 100, 500, 1000	Set the number of patterns to be averaged and measured in Differential Voltage Level Test and Pre-Emphasis Level Test.
Configure	Level VH Non Transition Location (HBR2CPAT)	LevelVHNonTransitionLocationHBR2CPAT	(Accepts user-defined text), 2.5, 5.5	Set the pattern bit location used for HBR2CPAT VH non transition measurement in Differential Voltage Level Test and Pre-Emphasis Level Test. Use comma separated location value, such as [x,y]. Where x is the start location, y is the end location.

**Table 2** Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Level VH Non Transition Location (Other Pattern)	LevelVHNonTransLocationOtherPattern	(Accepts user-defined text), 3.5, 6.5	Set the pattern bit location used for Other Pattern VH non transition measurement in Differential Voltage Level Test and Pre-Emphasis Level Test. Use comma separated location value, such as [x,y]. Where x is the start location, y is the end location.
Configure	Level VH Non Transition Location (PLTPAT)	LevelVHNonTransLocationPLTPAT	(Accepts user-defined text), 2.5, 5.5	Set the pattern bit location used for PLTPAT VH non transition measurement in Differential Voltage Level Test and Pre-Emphasis Level Test. Use comma separated location value, such as [x,y]. Where x is the start location, y is the end location.
Configure	Level VH Non Transition Location (PRBS 7)	LevelVHNonTransLocationPRBS7	(Accepts user-defined text), 3.5, 6.5	Set the pattern bit location used for PRBS 7 VH non transition measurement in Differential Voltage Level Test and Pre-Emphasis Level Test. Use comma separated location value, such as [x,y]. Where x is the start location, y is the end location.
Configure	Level VH Non Transition Location (PRBS 9)	LevelVHNonTransLocationPRBS9	(Accepts user-defined text), 3.5, 6.5	Set the pattern bit location used for PRBS 9 VH non transition measurement in Differential Voltage Level Test and Pre-Emphasis Level Test. Use comma separated location value, such as [x,y]. Where x is the start location, y is the end location.
Configure	Level VH Non Transition Location (Random Pattern)	LevelVHNonTransLocationRandomPattern	(Accepts user-defined text), 3.5, 6.5	Set the pattern bit location used for Random Pattern VH non transition measurement in Differential Voltage Level Test and Pre-Emphasis Level Test. Use comma separated location value, such as [x,y]. Where x is the start location, y is the end location.
Configure	Level VH Pattern (HBR2CPAT)	LevelVHPatternHBR2CPAT	(Accepts user-defined text), 011111	Set the triggering pattern used for HBR2CPAT VH measurement in Differential Voltage Level Test and Pre-Emphasis Level Test.
Configure	Level VH Pattern (Other Pattern)	LevelVHPatternOtherPattern	(Accepts user-defined text), 01111111	Set the triggering pattern used for Other Pattern VH measurement in Differential Voltage Level Test and Pre-Emphasis Level Test.

**Table 2** Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Level VH Pattern (PLTPAT)	LevelVHPattern PLTPAT	(Accepts user-defined text), 011111	Set the triggering pattern used for PLTPAT VH measurement in Differential Voltage Level Test and Pre-Emphasis Level Test.
Configure	Level VH Pattern (PRBS 7)	LevelVHPattern PRBS7	(Accepts user-defined text), 01111111	Set the triggering pattern used for PRBS 7 VH measurement in Differential Voltage Level Test and Pre-Emphasis Level Test.
Configure	Level VH Pattern (PRBS 9)	LevelVHPattern PRBS9	(Accepts user-defined text), 01111111	Set the triggering pattern used for PRBS 9 VH measurement in Differential Voltage Level Test and Pre-Emphasis Level Test.
Configure	Level VH Pattern (Random Pattern)	LevelVHPattern RandomPattern	(Accepts user-defined text), 01111111	Set the triggering pattern used for Random Pattern VH measurement in Differential Voltage Level Test and Pre-Emphasis Level Test.
Configure	Level VH Transition Location (HBR2CPAT)	LevelVHTransLocationHBR2CPAT	(Accepts user-defined text), 1.4, 1.7	Set the pattern bit location used for HBR2CPAT VH transition measurement in Differential Voltage Level Test and Pre-Emphasis Level Test. Use comma separated location value, such as [x,y]. Where x is the start location, y is the end location.
Configure	Level VH Transition Location (Other Pattern)	LevelVHTransLocationOtherPattern	(Accepts user-defined text), 1.4, 1.7	Set the pattern bit location used for Other Pattern VH transition measurement in Differential Voltage Level Test and Pre-Emphasis Level Test. Use comma separated location value, such as [x,y]. Where x is the start location, y is the end location.
Configure	Level VH Transition Location (PLTPAT)	LevelVHTransLocationPLTPAT	(Accepts user-defined text), 1.4, 1.7	Set the pattern bit location used for PLTPAT VH transition measurement in Differential Voltage Level Test and Pre-Emphasis Level Test. Use comma separated location value, such as [x,y]. Where x is the start location, y is the end location.

**Table 2** Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Level VH Transition Location (PRBS 7)	LevelVHTransitionPRBS7	(Accepts user-defined text), 1.4, 1.7	Set the pattern bit location used for PRBS 7 VH transition measurement in Differential Voltage Level Test and Pre-Emphasis Level Test. Use comma separated location value, such as [x,y]. Where x is the start location, y is the end location.
Configure	Level VH Transition Location (PRBS 9)	LevelVHTransitionPRBS9	(Accepts user-defined text), 1.4, 1.7	Set the pattern bit location used for PRBS 9 VH transition measurement in Differential Voltage Level Test and Pre-Emphasis Level Test. Use comma separated location value, such as [x,y]. Where x is the start location, y is the end location.
Configure	Level VH Transition Location (Random Pattern)	LevelVHTransitionRandomPattern	(Accepts user-defined text), 1.4, 1.7	Set the pattern bit location used for Random Pattern VH transition measurement in Differential Voltage Level Test and Pre-Emphasis Level Test. Use comma separated location value, such as [x,y]. Where x is the start location, y is the end location.
Configure	Level VL Non Transition Location (HBR2CPAT)	LevelVLNonTransitionLocationHBR2CPAT	(Accepts user-defined text), 4.5, 6.5	Set the pattern bit location used for HBR2CPAT VL non transition measurement in Differential Voltage Level Test and Pre-Emphasis Level Test. Use comma separated location value, such as [x,y]. Where x is the start location, y is the end location.
Configure	Level VL Non Transition Location (Other Pattern)	LevelVLNonTransitionLocationOtherPattern	(Accepts user-defined text), 4.5, 6.5	Set the pattern bit location used for Other Pattern VL non transition measurement in Differential Voltage Level Test and Pre-Emphasis Level Test. Use comma separated location value, such as [x,y]. Where x is the start location, y is the end location.
Configure	Level VL Non Transition Location (PLTPAT)	LevelVLNonTransitionLocationPLTPAT	(Accepts user-defined text), 2.5, 5.5	Set the pattern bit location used for PLTPAT VL non transition measurement in Differential Voltage Level Test and Pre-Emphasis Level Test. Use comma separated location value, such as [x,y]. Where x is the start location, y is the end location.



**Table 2** Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Level VL Non Transition Location (PRBS 7)	LevelVLNonTransLocationPRBS7	(Accepts user-defined text), 4.5, 6.5	Set the pattern bit location used for PRBS 7 VL non transition measurement in Differential Voltage Level Test and Pre-Emphasis Level Test. Use comma separated location value, such as [x,y]. Where x is the start location, y is the end location.
Configure	Level VL Non Transition Location (PRBS 9)	LevelVLNonTransLocationPRBS9	(Accepts user-defined text), 4.5, 6.5	Set the pattern bit location used for PRBS 9 VL non transition measurement in Differential Voltage Level Test and Pre-Emphasis Level Test. Use comma separated location value, such as [x,y]. Where x is the start location, y is the end location.
Configure	Level VL Non Transition Location (Random Pattern)	LevelVLNonTransLocationRandomPattern	(Accepts user-defined text), 4.5, 6.5	Set the pattern bit location used for Random Pattern VL non transition measurement in Differential Voltage Level Test and Pre-Emphasis Level Test. Use comma separated location value, such as [x,y]. Where x is the start location, y is the end location.
Configure	Level VL Pattern (HBR2CPAT)	LevelVLPatternHBR2CPAT	(Accepts user-defined text), 10100001	Set the triggering pattern used for HBR2CPAT VL measurement in Differential Voltage Level Test and Pre-Emphasis Level Test.
Configure	Level VL Pattern (Other Pattern)	LevelVLPatternOtherPattern	(Accepts user-defined text), 10100001	Set the triggering pattern used for Other Pattern VL measurement in Differential Voltage Level Test and Pre-Emphasis Level Test.
Configure	Level VL Pattern (PLTPAT)	LevelVLPatternPLTPAT	(Accepts user-defined text), 100000	Set the triggering pattern used for PLTPAT VL measurement in Differential Voltage Level Test and Pre-Emphasis Level Test.
Configure	Level VL Pattern (PRBS 7)	LevelVLPatternPRBS7	(Accepts user-defined text), 10100001	Set the triggering pattern used for PRBS 7 VL measurement in Differential Voltage Level Test and Pre-Emphasis Level Test.
Configure	Level VL Pattern (PRBS 9)	LevelVLPatternPRBS9	(Accepts user-defined text), 10100001	Set the triggering pattern used for PRBS 9 VL measurement in Differential Voltage Level Test and Pre-Emphasis Level Test.

**Table 2** Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Level VL Pattern (Random Pattern)	LevelVLPattern RandomPattern	(Accepts user-defined text), 10100001	Set the triggering pattern used for Random Pattern VL measurement in Differential Voltage Level Test and Pre-Emphasis Level Test.
Configure	Level VL Transition Location (HBR2CPAT)	LevelVLTransLo cationHBR2CP AT	(Accepts user-defined text), 3.4, 1.7	Set the pattern bit location used for HBR2CPAT VL transition measurement in Differential Voltage Level Test and Pre-Emphasis Level Test. Use comma separated location value, such as [x,y]. Where x is the start location, y is the end location.
Configure	Level VL Transition Location (Other Pattern)	LevelVLTransLo cationOtherPat tern	(Accepts user-defined text), 3.4, 3.7	Set the pattern bit location used for Other Pattern VL transition measurement in Differential Voltage Level Test and Pre-Emphasis Level Test. Use comma separated location value, such as [x,y]. Where x is the start location, y is the end location.
Configure	Level VL Transition Location (PLTPAT)	LevelVLTransLo cationPLTPAT	(Accepts user-defined text), 1.4, 1.7	Set the pattern bit location used for PLTPAT VL transition measurement in Differential Voltage Level Test and Pre-Emphasis Level Test. Use comma separated location value, such as [x,y]. Where x is the start location, y is the end location.
Configure	Level VL Transition Location (PRBS 7)	LevelVLTransLo cationPRBS7	(Accepts user-defined text), 3.4, 3.7	Set the pattern bit location used for PRBS 7 VL transition measurement in Differential Voltage Level Test and Pre-Emphasis Level Test. Use comma separated location value, such as [x,y]. Where x is the start location, y is the end location.
Configure	Level VL Transition Location (PRBS 9)	LevelVLTransLo cationPRBS9	(Accepts user-defined text), 3.4, 3.7	Set the pattern bit location used for PRBS 9 VL transition measurement in Differential Voltage Level Test and Pre-Emphasis Level Test. Use comma separated location value, such as [x,y]. Where x is the start location, y is the end location.

**Table 2** Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Level VL Transition Location (Random Pattern)	LevelVLTransLocationRandomPattern	(Accepts user-defined text), 3.4, 3.7	Set the pattern bit location used for Random Pattern VL transition measurement in Differential Voltage Level Test and Pre-Emphasis Level Test. Use comma separated location value, such as [x,y]. Where x is the start location, y is the end location.
Configure	Maximum Memory Depth (Mpts)	MaximumMemoryDepth	(Accepts user-defined text), 8.0, 10.0, 20.0, 30.0	Set the maximum memory depth limit for the acquisition setup of the oscilloscope. Unit: Mpts.
Configure	Maximum Sampling Rate (GSa/s)	MaximumSamplingRate	(Accepts user-defined text), 20.0, 40.0, 80.0	Set the maximum sampling rate for the acquisition setup of the oscilloscope. Unit: GSa/s.
Configure	Memory Depth (pts)	MemoryDepth	2050000, 5000000, 8000000	Set the memory depth for the acquisition setup of the oscilloscope. Unit: pts.
Configure	Pattern Check	EnableSignalCheck	1.0, 0.0	Select to enable or disable pattern checking. When pattern checking is enabled, the input signal is pre-tested and verified to be within a reasonable range of timing and voltage limits. This can be useful for detecting problems like cabling errors before a test is run.
Configure	Pattern Decode Method	PatternDecodeMethod	10, 1, 2	Select the method to decode the serial data pattern for pattern validation. For [Auto], [Method 1] is used for HBR2CPAT and equalizer and [Method 2] is used for other pattern. For [Method 1], waveform data is used to decode for serial data pattern. For [Method 2], TEdge measurement is used to decode for serial data pattern.
Configure	Probe External Scaling (Single-Ended)	ProbeExternalScalingSingleEnded	Disable, Enable	Select to enable or disable probe external scaling. For [Disable], the probe external scaling will be default to 0 before each run of the test. This configuration only applicable when Single-Ended connection type is used.
Configure	Prompt For AUX Traffic	PromptForAUXTraffic	true, false	Enable/Disable pop up to initiate traffic.
Configure	Rise Time Location (D10.2)	RiseTimeLocationD10_2	(Accepts user-defined text), 1	Set the zero based pattern bit location used for D10.2 rise time measurement in Rise Time Test.

**Table 2** Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Rise Time Location (HBR2CPAT)	RiseTimeLocationHBR2CPAT	(Accepts user-defined text), 1	Set the zero based pattern bit location used for HBR2CPAT rise time measurement in Rise Time Test.
Configure	Rise Time Location (Other Pattern)	RiseTimeLocationOtherPattern	(Accepts user-defined text), 1	Set the zero based pattern bit location used for Other Pattern rise time measurement in Rise Time Test.
Configure	Rise Time Location (PLTPAT)	RiseTimeLocationPLTPAT	(Accepts user-defined text), 1	Set the zero based pattern bit location used for PLTPAT rise time measurement in Rise Time Test.
Configure	Rise Time Location (PRBS 7)	RiseTimeLocationPRBS7	(Accepts user-defined text), 1	Set the zero based pattern bit location used for PRBS 7 rise time measurement in Rise Time Test.
Configure	Rise Time Location (PRBS 9)	RiseTimeLocationPRBS9	(Accepts user-defined text), 1	Set the zero based pattern bit location used for PRBS 9 rise time measurement in Rise Time Test.
Configure	Rise Time Location (Random Pattern)	RiseTimeLocationRandomPattern	(Accepts user-defined text), 1	Set the zero based pattern bit location used for Random Pattern rise time measurement in Rise Time Test.
Configure	Rise Time Pattern (D10.2)	RiseTimePatternD10_2	(Accepts user-defined text), 01	Set the triggering pattern used for D10.2 rise time measurement in Rise Time Test.
Configure	Rise Time Pattern (HBR2CPAT)	RiseTimePatternHBR2CPAT	(Accepts user-defined text), 01	Set the triggering pattern used for HBR2CPAT rise time measurement in Rise Time Test.
Configure	Rise Time Pattern (Other Pattern)	RiseTimePatternOtherPattern	(Accepts user-defined text), 01	Set the triggering pattern used for Other Pattern rise time measurement in Rise Time Test.
Configure	Rise Time Pattern (PLTPAT)	RiseTimePatternPLTPAT	(Accepts user-defined text), 011111	Set the triggering pattern used for PLTPAT rise time measurement in Rise Time Test.
Configure	Rise Time Pattern (PRBS 7)	RiseTimePatternPRBS7	(Accepts user-defined text), 01	Set the triggering pattern used for PRBS 7 rise time measurement in Rise Time Test.
Configure	Rise Time Pattern (PRBS 9)	RiseTimePatternPRBS9	(Accepts user-defined text), 01	Set the triggering pattern used for PRBS 9 rise time measurement in Rise Time Test.

**Table 2** Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Rise Time Pattern (Random Pattern)	RiseTimePatternRandomPattern	(Accepts user-defined text), 01	Set the triggering pattern used for Random Pattern rise time measurement in Rise Time Test.
Configure	SCPI Command Timeout	SCPITimeout	(Accepts user-defined text), 80000, 160000	Set the timeout period for SCPI command sent to oscilloscope in milliseconds. Unit: ms.
Configure	SSC Cycle Count	SSCCycleCount	(Accepts user-defined text), 10, 20	Set the number of SSC cycle captured and used for SSC related tests. Max number is 25.
Configure	SSC Filter Frequency (MHz)	SSCFilterFrequency	(Accepts user-defined text), 1.98, 1.70	Set the cutoff frequency of the low pass filter used for SSC related tests. Unit: MHz. This configuration only applicable when the [SSC Filter Type] config variable is set to [Second Order Butterworth Filter].
Configure	SSC Filter Type	SSCFilterType	SecondOrderButterworthFilter, SmoothingFilter	Select the type of the low pass filter used for SSC related tests.
Configure	SSC Smoothing Points - HBR	SSCSmoothingPointsHBR	(Accepts user-defined text), 61, 603, 701	Set the number of smoothing points of the low pass filter used for SSC related tests for HBR. This configuration only applicable when the [SSC Filter Type] config variable is set to [Smoothing Filter].
Configure	SSC Smoothing Points - HBR2	SSCSmoothingPointsHBR2	(Accepts user-defined text), 120, 1206, 1402	Set the number of smoothing points of the low pass filter used for SSC related tests for HBR2. This configuration only applicable when the [SSC Filter Type] config variable is set to [Smoothing Filter].
Configure	SSC Smoothing Points - HBR3	SSCSmoothingPointsHBR3	(Accepts user-defined text), 120, 1206, 1402	Set the number of smoothing points of the low pass filter used for SSC related tests for HBR3. This configuration only applicable when the [SSC Filter Type] config variable is set to [Smoothing Filter].
Configure	SSC Smoothing Points - RBR	SSCSmoothingPointsRBR	(Accepts user-defined text), 37, 361, 401	Set the number of smoothing points of the low pass filter used for SSC related tests for RBR. This configuration only applicable when the [SSC Filter Type] config variable is set to [Smoothing Filter].

**Table 2** Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Serial Data Pattern Method	SerialDataPatternMethod	1, 2	Set the method to search for serial data pattern for VHigh/VLow measurements. For [Method 1], Serial Data Pattern Qualify is used to search for serial data pattern. For [Method 2], InfiniiScan Generic Serial Trigger is used to search for serial data pattern.
Configure	Sink AUX Timeout(in us)	SinkAUXTimeout	(Accepts user-defined text), 300, 400	Set the time out period sink need to reply.
Configure	Source AUX Timeout(in us)	SourceAUXTimeout	(Accepts user-defined text), 300, 400	Set the time out period source need to wait for sink reply before transmitting the next AUX command.
Configure	Threshold Mode	ThresholdMode	Auto, Top Base, Min Max, Absolute Zero	Select the threshold mode for the measurement either VMax/VMin, VTop/VBase or Absolute Zero.
Configure	Transition Time Edges	TransitionTimeEdge	(Accepts user-defined text), 100, 500, 1000	Set the number of edges measured for Differential Transition Time Test.
Configure	Transition Time Memory Depth (kpts)	TransitionTimeMemoryDepth	(Accepts user-defined text), 100, 500, 1000	Set the memory depth for each acquisition in Differential Transition Time Test. Unit: kpts.
Configure	Transition Time Threshold	TransitionTimeThreshold	90/10, 85/15, 80/20, 75/25, 70/30	Set the threshold for the Differential Transition Time Test. Unit: Percentage.
Configure	Use Custom Transfer Function	CustomTransferFunction	True, False	De-embedding/Embedding using custom transfer function for TP3_EQ test if fixture de-embed is disable.
Configure	VH Pattern	VHPattern	1010111111, 101011111, 10101111	Set the pattern for VH measurement to either 1111110, 11110, 1110 or 110. The default setting is 1111110.
Configure	VL Pattern	VLPattern	1010000, 101000	Set the pattern for VL measurement to either 0000001, 00001, 0001 or 001. The default setting is 0000001.
Configure	VTop VBase Waveform Count	VTopVBaseWaveformCount	(Accepts user-defined text), 20, 50, 100	Set the number of waveforms used when performing the VTop and VBase measurement. Increasing this value increases the test run time but improves the repeatability of the measurement.
Run Tests	Event	RunEvent	(None), Fail, Margin < N, Pass	Names of events that can be used with the StoreMode=Event or RunUntil RunEventAction options

**Table 2** Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Run Tests	RunEvent=Margin < N: Minimum required margin %	RunEvent_Margin < N_MinPercent	Any integer in range: 0 <= value <= 100	Specify N using the 'Minimum required margin %' control.
Set Up	25Mhz < Dual Mode Clock < 165Mhz	DMPixelClockV 100	0.0, 1.0	Set when Dual Mode Clock Frequency is within 25Mhz and 165Mhz
Set Up	AUX Reference DUT	ReferenceDUT Connectivity	Yes, No	Define if a reference Source/DUT is attached during testing.
Set Up	AUX Waveform Type	AUXWaveformType	AUX Channel Tests, AUX Calibration Tests, AUX Sensitivity Tests	Define whether the waveform captured is for AUX Channel Tests or AUX Sensitivity Tests.
Set Up	Automated Test script	perTxtScript	(Accepts user-defined text)	Select a script for Automated Test
Set Up	Automated Tests Configuration	AutomationConfig	(Accepts user-defined text)	Configure the IP address and Port Number if W2642 DPTC is chosen. To do this, pass a string of 'IP=XXX.XXX.XXX.XXX / Port=XXXXX'.
Set Up	Automation Controller	AutomatedType	UnigrafDPTC, TCPIP	Select the controller used for automation. Select the controller used for automation.
Set Up	Automation Enable	pcbEnableAutomation	0.0, 1.0	Check to enable automation. Check to enable automation.
Set Up	Aux Acquisition Number:	perTxtAcquisitionNo	(Accepts user-defined text)	Number of waveform saved for offline processing.
Set Up	Aux Connection Type	AUXConnectionType	Differential Probe, Single-Ended	Define the connection type of AUX tests.
Set Up	Aux DUT Type	AUXDUTType	Source, Sink	Define the type of device being tested for AUX test suites.
Set Up	Aux Hold Off Time	perTxtHoldOffTime	(Accepts user-defined text)	Set the hold off time for AUX test acquisition
Set Up	Aux Lane	AuxLane	Channel 1, Channel 2, Channel 3, Channel 4	Set the channel used for differential Aux test signal.
Set Up	Aux Lower Threshold	perTxtAuxLowerThreshold	(Accepts user-defined text)	Define the lower threshold of AUX signals.
Set Up	Aux Offset	perTextOffset	(Accepts user-defined text)	Set the offset in mV for Aux Tests.

**Table 2** Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Aux Single-Ended Channel Scale	AUXSEChannelScale	(Accepts user-defined text)	Set the channel scale for each single-ended AUX lane channel. AUX+ and AUX- share the same scale.
Set Up	Aux Test Offline Mode	pcbOfflineMode	0.0, 1.0	Enable offline processing for Aux tests.
Set Up	Aux Trigger Level	perTxtTriggerLevel	(Accepts user-defined text)	Set the trigger level for Aux tests.
Set Up	Aux Upper Threshold	perTxtAuxUpperThreshold	(Accepts user-defined text)	Define the upper threshold of AUX signals.
Set Up	Aux Vertical Scale	perTxtVerticalScale	(Accepts user-defined text)	Set the vertical scale in mV for Aux Tests.
Set Up	Bit Rate 1	Bit Rate 1	0.0, 1.0	Enable/Disable bit rate 1 support.
Set Up	Bit Rate 2	Bit Rate 2	0.0, 1.0	Enable/Disable bit rate 2 support.
Set Up	Bit Rate 3	Bit Rate 3	0.0, 1.0	Enable/Disable bit rate 3 support.
Set Up	Bit Rate 4	Bit Rate 4	0.0, 1.0	Enable/Disable bit rate 4 support.
Set Up	Comments	Comments	(Accepts user-defined text)	Enter additional comments.
Set Up	Connection Type	ConnectionType	Differential Probe, Single-Ended (A-B)	Select the connection type to either Differential Probe or Single-Ended (A-B) connection.
Set Up	Connection Type	OfflineStep	Acquire, Run	Set the connection type to either Differential Probe or Single-Ended(A-B) connection
Set Up	DUT Connectivity(Sensitivity Calibration)	DUTConnectivity	Yes, No	Define if a DUT is used to cause traffic when calibrating aux channel prior to Aux sensitivity test.
Set Up	De-Embed Fixture	DeEmbedFixture	0.0, 1.0	Enable fixture de-embedding. Enable fixture de-embedding.
Set Up	Device Definition File Path	DeviceDefinitionFilePath	(Accepts user-defined text)	Set the path for Device Definition file to load. Set the path for Device Definition file to load.
Set Up	Device ID	DeviceID	(Accepts user-defined text)	Device identifier.
Set Up	Device Type	DeviceType	Source, Sink, Cable	Select the device type to either Source, Sink or Cable.
Set Up	Dual Mode Clk	DMClk	Channel 1, Channel 2, Channel 3, Channel 4	Set the channel used for Dual Mode Clk when using differential Probes



**Table 2** Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Dual Mode Clock >= 165Mhz	DMPixelClockV130	0.0, 1.0	Set when Dual Mode Clock Frequency is above 165Mhz
Set Up	Dual Mode Connection Type	DMConnectionType	(Accepts user-defined text), Single-Ended, Differential Probe	Define the connection type in Dual Mode Displayport.
Set Up	Dual Mode D0	DMD0	Channel 1, Channel 2, Channel 3, Channel 4	Set the channel used for Dual Mode D0 when using differential Probes
Set Up	Dual Mode D1	DMD1	Channel 1, Channel 2, Channel 4, Channel 3	Set the channel used for Dual Mode D1 when using differential Probes
Set Up	Dual Mode D2	DMD2	Channel 1, Channel 2, Channel 3, Channel 4	Set the channel used for Dual Mode D2 when using differential Probes
Set Up	Dual Mode Lane A for Differential probe connection.	DMLaneADiff	Clk	Select the corresponding Dual Mode Lane No when lane setting is set to 2 connections.
Set Up	Dual Mode Lane B for Differential probe connection.	DMLaneBDiff	D0, D1, D2	Select the corresponding Dual Mode Lane No when lane setting is set to 2 connections.
Set Up	Dual Mode No of Channels	DMConnectionChannels	2 Connections, 4 Connections	Define the number of channel connections for Dual Mode Displayport.
Set Up	Dual Mode Single Ended Lane A	DMLaneASMA	(Accepts user-defined text), Clk	Select the corresponding Lane No Dual Mode connection type is Singled-Ended.
Set Up	Dual Mode Single Ended Lane B	DMLaneBSMA	(Accepts user-defined text), D0, D1, D2	Select the corresponding Lane No Dual Mode connection type is Singled-Ended.
Set Up	Enable Offline mode for Physical Layer Tests.	pcbPhysicalLayerOfflineMode	0.0, 1.0	Enable Offline mode for Physical Layer Tests.
Set Up	Enable Test Plan	EnableTestPlan	0.0, 1.0	Enable or disable test plan.

**Table 2** Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Fixture Type	FixtureType	(Accepts user-defined text), Wilder Tech eDP-TPA30, Wilder Tech eDP-TPA40, Wilder Tech eDP-TPA50, Custom, None	Select the fixture type.
Set Up	Lane	Lane	1 Lane, 2 Lanes, 4 Lanes	Select the number of lanes for testing.
Set Up	Lane 0	Lane0	(Accepts user-defined text), Channel 1, Channel 2, Channel 3, Channel 4	Set the channel used for Lane 0 when using differential Probes
Set Up	Lane 1	Lane1	(Accepts user-defined text), Channel 1, Channel 2, Channel 3, Channel 4	Set the channel used for Lane 1 when using differential Probes
Set Up	Lane 2	Lane2	(Accepts user-defined text), Channel 1, Channel 2, Channel 3, Channel 4	Set the channel used for Lane 2 when using differential Probes
Set Up	Lane 3	Lane3	(Accepts user-defined text), Channel 1, Channel 2, Channel 3, Channel 4	Set the channel used for Lane 3 when using differential Probes
Set Up	Lane A(2 Lanes)	LaneA_4	(Accepts user-defined text), Lane 0, Lane 1	Select the corresponding Lane No when lane setting is set to 2 Lanes.
Set Up	Lane A(4 Lanes)	LaneA	(Accepts user-defined text), Lane 0, Lane 1, Lane 2, Lane 3	Select the corresponding Lane No when lane setting is set to 4 Lanes.
Set Up	Lane B(4 Lanes)	LaneB	(Accepts user-defined text), Lane 0, Lane 1, Lane 2, Lane 3	Select the corresponding Lane No when lane setting is set to 4 Lanes.
Set Up	Last Test ID	LastTestIDRun	(Accepts user-defined text)	Retrieve Test ID of last test run.
Set Up	Level Swing 0	Swing 0	0.0, 1.0	Enable/Disable Swing 0 support
Set Up	Level Swing 1	Swing 1	0.0, 1.0	Enable/Disable Swing 1 support
Set Up	Level Swing 2	Swing 2	0.0, 1.0	Enable/Disable Swing 2 support
Set Up	Level Swing 3	Swing 3	0.0, 1.0	Enable/Disable Swing 3 support
Set Up	No of Channels	ConnectionSetting	1 Channel, 2 Channels, 4 Channels	Number of channels to be used.
Set Up	No of Channels (Differential Probe Connections)	ConnectionSettingDiff	(Accepts user-defined text), 1 Channel, 2 Channels, 4 Channels	Set the number of channels to be used for differential probe connection. Set the number of channels to be used for differential probe connection.

**Table 2** Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	No of Channels (Single-Ended Connections)	ConnectionSettingSingleEnded	(Accepts user-defined text), 2 Channels, 4 Channels	Set the number of channels to be used for single-ended connection. Set the number of channels to be used for single-ended connection.
Set Up	Operator ID	OperatorID	(Accepts user-defined text)	Operator identifier.
Set Up	Post Cursor2 Level 0	Level 0	0.0, 1.0	Enable/Disable PostCursor2 Level 0 support.
Set Up	Post Cursor2 Level 1	Level 1	0.0, 1.0	Enable/Disable PostCursor2 Level 1 support.
Set Up	Post Cursor2 Level 2	Level 2	0.0, 1.0	Enable/Disable PostCursor2 Level 2 support.
Set Up	Post Cursor2 Level 3	Level 3	0.0, 1.0	Enable/Disable PostCursor2 Level 3 support.
Set Up	Pre-emphasis 0	Pre-emphasis 0	0.0, 1.0	Enable/Disable Pre-emphasis 0 support
Set Up	Pre-emphasis 1	Pre-emphasis 1	0.0, 1.0	Enable/Disable Pre-emphasis 1 support
Set Up	Pre-emphasis 2	Pre-emphasis 2	0.0, 1.0	Enable/Disable Pre-emphasis 2 support
Set Up	Pre-emphasis 3	Pre-emphasis 3	0.0, 1.0	Enable/Disable Pre-emphasis 3 support
Set Up	Probe+ Offset	ProbePlusOffset	(Accepts user-defined text)	Set the probe offset for AUX+ channel
Set Up	Probe- Offset	ProbeMinusOffset	(Accepts user-defined text)	Set the probe offset for AUX- channel.
Set Up	Project ID	ProjectID	(Accepts user-defined text)	Project identifier.
Set Up	Show Normative Tests Only	HideInformative	0.0, 1.0	Show normative tests only.
Set Up	Single Ended Lane A(2 Lanes)	LaneASMA_4	(Accepts user-defined text), Lane 0, Lane 1	Select the corresponding Lane No when lane setting is set to 2 Lanes and connection type is Singled-Ended.
Set Up	Single Ended Lane A(4 Lanes)	LaneASMA	(Accepts user-defined text), Lane 0, Lane 1, Lane 2, Lane 3	Select the corresponding Lane No when lane setting is set to 4 Lanes and connection type is Singled-Ended
Set Up	Single Ended Lane B(4 Lanes)	LaneBSMA	(Accepts user-defined text), Lane 0, Lane 1, Lane 2, Lane 3	Select the corresponding Lane No when lane setting is set to 4 Lanes and connection type is Singled-Ended.
Set Up	Single Ended Lane0Minus	DMD0Minus	Channel 4, Channel 3	Set the channel used for Lane 0- when using Single-Ended Connection.

**Table 2** Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Single Ended Lane0Minus	Lane0Minus	(Accepts user-defined text), Channel 3, Channel 4	Set the channel used for Lane 0- when using Single-Ended Connection.
Set Up	Single Ended Lane0Plus	DMD0Plus	Channel 1, Channel 2	Set the channel used for Lane 0+ when using Single-Ended Connection.
Set Up	Single Ended Lane0Plus	Lane0Plus	(Accepts user-defined text), Channel 1, Channel 2	Set the channel used for Lane 0+ when using Single-Ended Connection.
Set Up	Single Ended Lane1Minus	DMD1Minus	Channel 4, Channel 3	Set the channel used for Lane 1- when using Single-Ended Connection.
Set Up	Single Ended Lane1Minus	Lane1Minus	(Accepts user-defined text), Channel 3, Channel 4	Set the channel used for Lane 1- when using Single-Ended Connection.
Set Up	Single Ended Lane1Plus	DMD1Plus	Channel 2, Channel 1	Set the channel used for Lane 1+ when using Single-Ended Connection.
Set Up	Single Ended Lane1Plus	Lane1Plus	(Accepts user-defined text), Channel 1, Channel 2	Set the channel used for Lane 1+ when using Single-Ended Connection.
Set Up	Single Ended Lane2Minus	DMD2Minus	Channel 4, Channel 3	Set the channel used for Lane 2- when using Single-Ended Connection.
Set Up	Single Ended Lane2Minus	Lane2Minus	(Accepts user-defined text), Channel 3, Channel 4	Set the channel used for Lane 2- when using Single-Ended Connection.
Set Up	Single Ended Lane2Plus	DMD2Plus	Channel 2, Channel 1	Set the channel used for Lane 2+ when using Single-Ended Connection.
Set Up	Single Ended Lane2Plus	Lane2Plus	(Accepts user-defined text), Channel 1, Channel 2	Set the channel used for Lane 2+ when using Single-Ended Connection.
Set Up	Single Ended Lane3Minus	DMClkMinus	Channel 3, Channel 4	Set the channel used for Lane 3- when using Single-Ended Connection.
Set Up	Single Ended Lane3Minus	Lane3Minus	(Accepts user-defined text), Channel 3, Channel 4	Set the channel used for Lane 3- when using Single-Ended Connection.
Set Up	Single Ended Lane3Plus	DMClkPlus	Channel 1, Channel 2	Set the channel used for Lane 3+ when using Single-Ended Connection.
Set Up	Single Ended Lane3Plus	Lane3Plus	(Accepts user-defined text), Channel 1, Channel 2	Set the channel used for Lane 3+ when using Single-Ended Connection.
Set Up	Switch Matrix Enable	SwitchMatrixEnable	0.0, 1.0	Check to enable switch matrix.
Set Up	Test Layer	TestSelection	Physical Layer Tests, Aux Channel Physical Layer Tests, Utility Tests	

**Table 2** Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Test Mode	TestMode	Compliance Conditions Only, User Defined Conditions, Targeted Characterization Testing	Three test modes are allowed for display port (Compliance Conditions Only, User Defined Conditions and Targeted Characterization Testing mode).
Set Up	Test Specification	DPCTSVersion	eDP 1.4, eDP 1.3	Select test specification.
Set Up	Test Type	TestType	Differential Tests, Single-Ended Tests, Both	Select the test type to either Differential Tests, Single-Ended Tests or Both if the device type is Source.
Set Up	Update Controls	UpdateList	0.0, 1.0	Set this to 1.0 to trigger an event to update all controls and settings.

## 2 Configuration Variables and Values

## 3 Test Names and IDs

The following table shows the mapping between each test's numeric ID and name. The numeric ID is required by various remote interface methods.

- Name – The name of the test as it appears on the user interface **Select Tests** tab.
- Test ID – The number to use with the RunTests method.
- Description – The description of the test as it appears on the user interface **Select Tests** tab.

For example, if the graphical user interface displays this tree in the **Select Tests** tab:

- All Tests
  - Rise Time
  - Fall Time

then you would expect to see something like this in the table below:

**Table 3** Example Test Names and IDs

Name	Test ID	Description
Fall Time	110	Measures clock fall time.
Rise Time	100	Measures clock rise time.

and you would run these tests remotely using:

ARSL syntax

-----

```
arsl -a ipaddress -c "SelectedTests '100,110'"  
arsl -a ipaddress -c "Run"
```

C# syntax

-----

```
remoteAte.SelectedTests = new int[] {100,110};  
remoteAte.Run();
```

Here are the actual Test names and IDs used by this application:

**NOTE**

The file, "TestInfo.txt", which may be found in the same directory as this help file, contains all of the information found in the table below in a format suitable for parsing.

**Table 4** Test IDs and Names

Name	TestID	Description
Clock Recovery Settings	1201	
Configurable Parameter Settings	1200	
Eye Diagram Settings	105	
Jitter Settings	106	
Lane 0 - AC Common Mode Noise Test (HBR2CPAT)	510201	To report common mode noise (unfiltered RMS) of the differential pairs of the eDP interface. These measurements can be useful in predicting the channels EMI/RFI performance.
Lane 0 - Deterministic Jitter Test (TP3_EQ) (D10.2)	43201	To evaluate the Deterministic Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 0 - Deterministic Jitter Test (TP3_EQ) (HBR2CPAT)	40201	To evaluate the Deterministic Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 0 - Deterministic Jitter Test (TP3_EQ) (Other Pattern)	49201	To evaluate the Deterministic Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 0 - Deterministic Jitter Test (TP3_EQ) (PRBS 7)	41201	To evaluate the Deterministic Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 0 - Deterministic Jitter Test (TP3_EQ) (PRBS 9)	42201	To evaluate the Deterministic Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.



**Table 4** Test IDs and Names (continued)

Name	TestID	Description
Lane 0 - Deterministic Jitter Test (TP3_EQ) (Random Pattern)	48201	To evaluate the Deterministic Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 0 - Differential Voltage Level Test (HBR2CPAT)	70201	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 0 - Differential Voltage Level Test (HBR2CPAT)	80201	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 0 - Differential Voltage Level Test (Other Pattern)	79201	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 0 - Differential Voltage Level Test (Other Pattern)	89201	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 0 - Differential Voltage Level Test (PLTPAT)	74201	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 0 - Differential Voltage Level Test (PLTPAT)	84201	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 0 - Differential Voltage Level Test (PRBS 7)	71201	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 0 - Differential Voltage Level Test (PRBS 7)	81201	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 0 - Differential Voltage Level Test (PRBS 9)	72201	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 0 - Differential Voltage Level Test (PRBS 9)	82201	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 0 - Differential Voltage Level Test (Random Pattern)	78201	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 0 - Differential Voltage Level Test (Random Pattern)	88201	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 0 - Eye Diagram Test (TP3_EQ) (D10.2)	13201	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
Lane 0 - Eye Diagram Test (TP3_EQ) (HBR2CPAT)	10201	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.

**Table 4** Test IDs and Names (continued)

Name	TestID	Description
Lane 0 - Eye Diagram Test (TP3_EQ) (Other Pattern)	19201	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
Lane 0 - Eye Diagram Test (TP3_EQ) (PRBS 7)	11201	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
Lane 0 - Eye Diagram Test (TP3_EQ) (PRBS 9)	12201	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
Lane 0 - Eye Diagram Test (TP3_EQ) (Random Pattern)	18201	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
Lane 0 - Fall Time Test (D10.2)	123201	To evaluate the differential fall time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 0 - Fall Time Test (HBR2CPAT)	120201	To evaluate the differential fall time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 0 - Fall Time Test (Other Pattern)	129201	To evaluate the differential fall time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 0 - Fall Time Test (PLTPAT)	124201	To evaluate the differential fall time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 0 - Fall Time Test (PRBS 7)	121201	To evaluate the differential fall time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 0 - Fall Time Test (PRBS 9)	122201	To evaluate the differential fall time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.

**Table 4** Test IDs and Names (continued)

Name	TestID	Description
Lane 0 - Fall Time Test (Random Pattern)	128201	To evaluate the differential fall time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 0 - Intra Pair Skew Test (D10.2)	503201	To evaluate the skew, or time delay, between the n and p legs of the differential pairs of the eDP interface. These measurements can be useful in predicting the channels EMI/RFI performance.
Lane 0 - Intra Pair Skew Test (HBR2CPAT)	500201	To evaluate the skew, or time delay, between the n and p legs of the differential pairs of the eDP interface. These measurements can be useful in predicting the channels EMI/RFI performance.
Lane 0 - Main Link Frequency Compliance Test (D10.2)	203201	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 0 - Main Link Frequency Compliance Test (D10.2)	253201	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 0 - Main Link Frequency Compliance Test (HBR2CPAT)	200201	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 0 - Main Link Frequency Compliance Test (HBR2CPAT)	250201	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 0 - Main Link Frequency Compliance Test (Other Pattern)	209201	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 0 - Main Link Frequency Compliance Test (Other Pattern)	259201	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 0 - Main Link Frequency Compliance Test (PRBS 7)	201201	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 0 - Main Link Frequency Compliance Test (PRBS 7)	251201	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 0 - Main Link Frequency Compliance Test (PRBS 9)	202201	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.

**Table 4** Test IDs and Names (continued)

Name	TestID	Description
Lane 0 - Main Link Frequency Compliance Test (PRBS 9)	252201	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 0 - Main Link Frequency Compliance Test (Random Pattern)	208201	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 0 - Main Link Frequency Compliance Test (Random Pattern)	258201	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 0 - Non ISI Jitter Test (D10.2)	23201	To evaluate the amount of eDP Non ISI jitter accompanying the data transmission.
Lane 0 - Non ISI Jitter Test (HBR2CPAT)	20201	To evaluate the amount of eDP Non ISI jitter accompanying the data transmission.
Lane 0 - Non ISI Jitter Test (Other Pattern)	29201	To evaluate the amount of eDP Non ISI jitter accompanying the data transmission.
Lane 0 - Non ISI Jitter Test (PRBS 7)	21201	To evaluate the amount of eDP Non ISI jitter accompanying the data transmission.
Lane 0 - Non ISI Jitter Test (PRBS 9)	22201	To evaluate the amount of eDP Non ISI jitter accompanying the data transmission.
Lane 0 - Non ISI Jitter Test (Random Pattern)	28201	To evaluate the amount of eDP Non ISI jitter accompanying the data transmission.
Lane 0 - Peak to Peak Differential Voltage Test (HBR2CPAT)	60201	To evaluate the peak to peak differential voltage of the DUT's transmitted signal is within the conformance limits.
Lane 0 - Peak to Peak Differential Voltage Test (Other Pattern)	69201	To evaluate the peak to peak differential voltage of the DUT's transmitted signal is within the conformance limits.
Lane 0 - Peak to Peak Differential Voltage Test (PLTPAT)	64201	To evaluate the peak to peak differential voltage of the DUT's transmitted signal is within the conformance limits.
Lane 0 - Peak to Peak Differential Voltage Test (PRBS 7)	61201	To evaluate the peak to peak differential voltage of the DUT's transmitted signal is within the conformance limits.
Lane 0 - Peak to Peak Differential Voltage Test (PRBS 9)	62201	To evaluate the peak to peak differential voltage of the DUT's transmitted signal is within the conformance limits.
Lane 0 - Peak to Peak Differential Voltage Test (Random Pattern)	68201	To evaluate the peak to peak differential voltage of the DUT's transmitted signal is within the conformance limits.

**Table 4** Test IDs and Names (continued)

Name	TestID	Description
Lane 0 - Pre-Emphasis Level Test (HBR2CPAT)	90201	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 0 - Pre-Emphasis Level Test (HBR2CPAT)	100201	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 0 - Pre-Emphasis Level Test (Other Pattern)	99201	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 0 - Pre-Emphasis Level Test (Other Pattern)	109201	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 0 - Pre-Emphasis Level Test (PLTPAT)	94201	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 0 - Pre-Emphasis Level Test (PLTPAT)	104201	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 0 - Pre-Emphasis Level Test (PRBS 7)	91201	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 0 - Pre-Emphasis Level Test (PRBS 7)	101201	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 0 - Pre-Emphasis Level Test (PRBS 9)	92201	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 0 - Pre-Emphasis Level Test (PRBS 9)	102201	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 0 - Pre-Emphasis Level Test (Random Pattern)	98201	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 0 - Pre-Emphasis Level Test (Random Pattern)	108201	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 0 - Random Jitter Test (TP3_EQ) (D10.2)	53201	To evaluate the Random Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 0 - Random Jitter Test (TP3_EQ) (HBR2CPAT)	50201	To evaluate the Random Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 0 - Random Jitter Test (TP3_EQ) (Other Pattern)	59201	To evaluate the Random Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.

**Table 4** Test IDs and Names (continued)

Name	TestID	Description
Lane 0 - Random Jitter Test (TP3_EQ) (PRBS 7)	51201	To evaluate the Random Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 0 - Random Jitter Test (TP3_EQ) (PRBS 9)	52201	To evaluate the Random Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 0 - Random Jitter Test (TP3_EQ) (Random Pattern)	58201	To evaluate the Random Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 0 - Rise Time Test (D10.2)	113201	To evaluate the differential rise time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 0 - Rise Time Test (HBR2CPAT)	110201	To evaluate the differential rise time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 0 - Rise Time Test (Other Pattern)	119201	To evaluate the differential rise time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 0 - Rise Time Test (PLTPAT)	114201	To evaluate the differential rise time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 0 - Rise Time Test (PRBS 7)	111201	To evaluate the differential rise time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 0 - Rise Time Test (PRBS 9)	112201	To evaluate the differential rise time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 0 - Rise Time Test (Random Pattern)	118201	To evaluate the differential rise time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.

**Table 4** Test IDs and Names (continued)

Name	TestID	Description
Lane 0 - SSC Modulation Deviation Test (D10.2)	353201	To evaluate the range of SSC down-spreading of the DUT's transmitted signal in ppm is within the conformance limits.
Lane 0 - SSC Modulation Deviation Test (HBR2CPAT)	350201	To evaluate the range of SSC down-spreading of the DUT's transmitted signal in ppm is within the conformance limits.
Lane 0 - SSC Modulation Deviation Test (Other Pattern)	359201	To evaluate the range of SSC down-spreading of the DUT's transmitted signal in ppm is within the conformance limits.
Lane 0 - SSC Modulation Deviation Test (PRBS 7)	351201	To evaluate the range of SSC down-spreading of the DUT's transmitted signal in ppm is within the conformance limits.
Lane 0 - SSC Modulation Deviation Test (PRBS 9)	352201	To evaluate the range of SSC down-spreading of the DUT's transmitted signal in ppm is within the conformance limits.
Lane 0 - SSC Modulation Deviation Test (Random Pattern)	358201	To evaluate the range of SSC down-spreading of the DUT's transmitted signal in ppm is within the conformance limits.
Lane 0 - SSC Modulation Frequency Test (D10.2)	303201	To evaluate the frequency of the SSC modulation and to validate it falls with specification limits.
Lane 0 - SSC Modulation Frequency Test (HBR2CPAT)	300201	To evaluate the frequency of the SSC modulation and to validate it falls with specification limits.
Lane 0 - SSC Modulation Frequency Test (Other Pattern)	309201	To evaluate the frequency of the SSC modulation and to validate it falls with specification limits.
Lane 0 - SSC Modulation Frequency Test (PRBS 7)	301201	To evaluate the frequency of the SSC modulation and to validate it falls with specification limits.
Lane 0 - SSC Modulation Frequency Test (PRBS 9)	302201	To evaluate the frequency of the SSC modulation and to validate it falls with specification limits.
Lane 0 - SSC Modulation Frequency Test (Random Pattern)	308201	To evaluate the frequency of the SSC modulation and to validate it falls with specification limits.
Lane 0 - Total Jitter Test (TP3_EQ) (D10.2)	33201	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.

**Table 4** Test IDs and Names (continued)

Name	TestID	Description
Lane 0 - Total Jitter Test (TP3_EQ) (HBR2CPAT)	30201	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 0 - Total Jitter Test (TP3_EQ) (Other Pattern)	39201	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 0 - Total Jitter Test (TP3_EQ) (PRBS 7)	31201	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 0 - Total Jitter Test (TP3_EQ) (PRBS 9)	32201	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 0 - Total Jitter Test (TP3_EQ) (Random Pattern)	38201	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 0 / Lane 1 - Inter Pair Skew Test (HBR2CPAT)	130201	To evaluate the skew, or time delay, between differential main link data lanes of the eDP interface.
Lane 0 / Lane 1 - Inter Pair Skew Test (Other Pattern)	139201	To evaluate the skew, or time delay, between differential main link data lanes of the eDP interface.
Lane 0 / Lane 1 - Inter Pair Skew Test (PRBS 7)	131201	To evaluate the skew, or time delay, between differential main link data lanes of the eDP interface.
Lane 0 / Lane 1 - Inter Pair Skew Test (PRBS 9)	132201	To evaluate the skew, or time delay, between differential main link data lanes of the eDP interface.
Lane 0 / Lane 1 - Inter Pair Skew Test (Random Pattern)	138201	To evaluate the skew, or time delay, between differential main link data lanes of the eDP interface.
Lane 0 / Lane 2 - Inter Pair Skew Test (HBR2CPAT)	130202	To evaluate the skew, or time delay, between differential main link data lanes of the eDP interface.
Lane 0 / Lane 2 - Inter Pair Skew Test (Other Pattern)	139202	To evaluate the skew, or time delay, between differential main link data lanes of the eDP interface.
Lane 0 / Lane 2 - Inter Pair Skew Test (PRBS 7)	131202	To evaluate the skew, or time delay, between differential main link data lanes of the eDP interface.



**Table 4** Test IDs and Names (continued)

Name	TestID	Description
Lane 0 / Lane 2 - Inter Pair Skew Test (PRBS 9)	132202	To evaluate the skew, or time delay, between differential main link data lanes of the eDP interface.
Lane 0 / Lane 2 - Inter Pair Skew Test (Random Pattern)	138202	To evaluate the skew, or time delay, between differential main link data lanes of the eDP interface.
Lane 0 / Lane 3 - Inter Pair Skew Test (HBR2CPAT)	130203	To evaluate the skew, or time delay, between differential main link data lanes of the eDP interface.
Lane 0 / Lane 3 - Inter Pair Skew Test (Other Pattern)	139203	To evaluate the skew, or time delay, between differential main link data lanes of the eDP interface.
Lane 0 / Lane 3 - Inter Pair Skew Test (PRBS 7)	131203	To evaluate the skew, or time delay, between differential main link data lanes of the eDP interface.
Lane 0 / Lane 3 - Inter Pair Skew Test (PRBS 9)	132203	To evaluate the skew, or time delay, between differential main link data lanes of the eDP interface.
Lane 0 / Lane 3 - Inter Pair Skew Test (Random Pattern)	138203	To evaluate the skew, or time delay, between differential main link data lanes of the eDP interface.
Lane 1 - AC Common Mode Noise Test (HBR2CPAT)	510202	To report common mode noise (unfiltered RMS) of the differential pairs of the eDP interface. These measurements can be useful in predicting the channels EMI/RFI performance.
Lane 1 - Deterministic Jitter Test (TP3_EQ) (D10.2)	43202	To evaluate the Deterministic Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 1 - Deterministic Jitter Test (TP3_EQ) (HBR2CPAT)	40202	To evaluate the Deterministic Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 1 - Deterministic Jitter Test (TP3_EQ) (Other Pattern)	49202	To evaluate the Deterministic Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 1 - Deterministic Jitter Test (TP3_EQ) (PRBS 7)	41202	To evaluate the Deterministic Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.

**Table 4** Test IDs and Names (continued)

Name	TestID	Description
Lane 1 - Deterministic Jitter Test (TP3_EQ) (PRBS 9)	42202	To evaluate the Deterministic Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 1 - Deterministic Jitter Test (TP3_EQ) (Random Pattern)	48202	To evaluate the Deterministic Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 1 - Differential Voltage Level Test (HBR2CPAT)	70202	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 1 - Differential Voltage Level Test (HBR2CPAT)	80202	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 1 - Differential Voltage Level Test (Other Pattern)	79202	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 1 - Differential Voltage Level Test (Other Pattern)	89202	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 1 - Differential Voltage Level Test (PLTPAT)	74202	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 1 - Differential Voltage Level Test (PLTPAT)	84202	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 1 - Differential Voltage Level Test (PRBS 7)	71202	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 1 - Differential Voltage Level Test (PRBS 7)	81202	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 1 - Differential Voltage Level Test (PRBS 9)	72202	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 1 - Differential Voltage Level Test (PRBS 9)	82202	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 1 - Differential Voltage Level Test (Random Pattern)	78202	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 1 - Differential Voltage Level Test (Random Pattern)	88202	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 1 - Eye Diagram Test (TP3_EQ) (D10.2)	13202	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.

**Table 4** Test IDs and Names (continued)

Name	TestID	Description
Lane 1 - Eye Diagram Test (TP3_EQ) (HBR2CPAT)	10202	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
Lane 1 - Eye Diagram Test (TP3_EQ) (Other Pattern)	19202	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
Lane 1 - Eye Diagram Test (TP3_EQ) (PRBS 7)	11202	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
Lane 1 - Eye Diagram Test (TP3_EQ) (PRBS 9)	12202	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
Lane 1 - Eye Diagram Test (TP3_EQ) (Random Pattern)	18202	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
Lane 1 - Fall Time Test (D10.2)	123202	To evaluate the differential fall time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 1 - Fall Time Test (HBR2CPAT)	120202	To evaluate the differential fall time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 1 - Fall Time Test (Other Pattern)	129202	To evaluate the differential fall time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 1 - Fall Time Test (PLTPAT)	124202	To evaluate the differential fall time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 1 - Fall Time Test (PRBS 7)	121202	To evaluate the differential fall time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.

**Table 4** Test IDs and Names (continued)

Name	TestID	Description
Lane 1 - Fall Time Test (PRBS 9)	122202	To evaluate the differential fall time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 1 - Fall Time Test (Random Pattern)	128202	To evaluate the differential fall time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 1 - Intra Pair Skew Test (D10.2)	503202	To evaluate the skew, or time delay, between the n and p legs of the differential pairs of the eDP interface. These measurements can be useful in predicting the channels EMI/RFI performance.
Lane 1 - Intra Pair Skew Test (HBR2CPAT)	500202	To evaluate the skew, or time delay, between the n and p legs of the differential pairs of the eDP interface. These measurements can be useful in predicting the channels EMI/RFI performance.
Lane 1 - Main Link Frequency Compliance Test (D10.2)	203202	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 1 - Main Link Frequency Compliance Test (D10.2)	253202	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 1 - Main Link Frequency Compliance Test (HBR2CPAT)	200202	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 1 - Main Link Frequency Compliance Test (HBR2CPAT)	250202	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 1 - Main Link Frequency Compliance Test (Other Pattern)	209202	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 1 - Main Link Frequency Compliance Test (Other Pattern)	259202	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 1 - Main Link Frequency Compliance Test (PRBS 7)	201202	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 1 - Main Link Frequency Compliance Test (PRBS 7)	251202	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.

**Table 4** Test IDs and Names (continued)

Name	TestID	Description
Lane 1 - Main Link Frequency Compliance Test (PRBS 9)	202202	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 1 - Main Link Frequency Compliance Test (PRBS 9)	252202	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 1 - Main Link Frequency Compliance Test (Random Pattern)	208202	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 1 - Main Link Frequency Compliance Test (Random Pattern)	258202	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 1 - Non ISI Jitter Test (D10.2)	23202	To evaluate the amount of eDP Non ISI jitter accompanying the data transmission.
Lane 1 - Non ISI Jitter Test (HBR2CPAT)	20202	To evaluate the amount of eDP Non ISI jitter accompanying the data transmission.
Lane 1 - Non ISI Jitter Test (Other Pattern)	29202	To evaluate the amount of eDP Non ISI jitter accompanying the data transmission.
Lane 1 - Non ISI Jitter Test (PRBS 7)	21202	To evaluate the amount of eDP Non ISI jitter accompanying the data transmission.
Lane 1 - Non ISI Jitter Test (PRBS 9)	22202	To evaluate the amount of eDP Non ISI jitter accompanying the data transmission.
Lane 1 - Non ISI Jitter Test (Random Pattern)	28202	To evaluate the amount of eDP Non ISI jitter accompanying the data transmission.
Lane 1 - Peak to Peak Differential Voltage Test (HBR2CPAT)	60202	To evaluate the peak to peak differential voltage of the DUT's transmitted signal is within the conformance limits.
Lane 1 - Peak to Peak Differential Voltage Test (Other Pattern)	69202	To evaluate the peak to peak differential voltage of the DUT's transmitted signal is within the conformance limits.
Lane 1 - Peak to Peak Differential Voltage Test (PLTPAT)	64202	To evaluate the peak to peak differential voltage of the DUT's transmitted signal is within the conformance limits.
Lane 1 - Peak to Peak Differential Voltage Test (PRBS 7)	61202	To evaluate the peak to peak differential voltage of the DUT's transmitted signal is within the conformance limits.
Lane 1 - Peak to Peak Differential Voltage Test (PRBS 9)	62202	To evaluate the peak to peak differential voltage of the DUT's transmitted signal is within the conformance limits.

**Table 4** Test IDs and Names (continued)

Name	TestID	Description
Lane 1 - Peak to Peak Differential Voltage Test (Random Pattern)	68202	To evaluate the peak to peak differential voltage of the DUT's transmitted signal is within the conformance limits.
Lane 1 - Pre-Emphasis Level Test (HBR2CPAT)	90202	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 1 - Pre-Emphasis Level Test (HBR2CPAT)	100202	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 1 - Pre-Emphasis Level Test (Other Pattern)	99202	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 1 - Pre-Emphasis Level Test (Other Pattern)	109202	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 1 - Pre-Emphasis Level Test (PLTPAT)	94202	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 1 - Pre-Emphasis Level Test (PLTPAT)	104202	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 1 - Pre-Emphasis Level Test (PRBS 7)	91202	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 1 - Pre-Emphasis Level Test (PRBS 7)	101202	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 1 - Pre-Emphasis Level Test (PRBS 9)	92202	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 1 - Pre-Emphasis Level Test (PRBS 9)	102202	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 1 - Pre-Emphasis Level Test (Random Pattern)	98202	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 1 - Pre-Emphasis Level Test (Random Pattern)	108202	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 1 - Random Jitter Test (TP3_EQ) (D10.2)	53202	To evaluate the Random Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 1 - Random Jitter Test (TP3_EQ) (HBR2CPAT)	50202	To evaluate the Random Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.

**Table 4** Test IDs and Names (continued)

Name	TestID	Description
Lane 1 - Random Jitter Test (TP3_EQ) (Other Pattern)	59202	To evaluate the Random Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 1 - Random Jitter Test (TP3_EQ) (PRBS 7)	51202	To evaluate the Random Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 1 - Random Jitter Test (TP3_EQ) (PRBS 9)	52202	To evaluate the Random Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 1 - Random Jitter Test (TP3_EQ) (Random Pattern)	58202	To evaluate the Random Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 1 - Rise Time Test (D10.2)	113202	To evaluate the differential rise time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 1 - Rise Time Test (HBR2CPAT)	110202	To evaluate the differential rise time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 1 - Rise Time Test (Other Pattern)	119202	To evaluate the differential rise time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 1 - Rise Time Test (PLTPAT)	114202	To evaluate the differential rise time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 1 - Rise Time Test (PRBS 7)	111202	To evaluate the differential rise time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.

**Table 4** Test IDs and Names (continued)

Name	TestID	Description
Lane 1 - Rise Time Test (PRBS 9)	112202	To evaluate the differential rise time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 1 - Rise Time Test (Random Pattern)	118202	To evaluate the differential rise time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 1 - SSC Modulation Deviation Test (D10.2)	353202	To evaluate the range of SSC down-spreading of the DUT's transmitted signal in ppm is within the conformance limits.
Lane 1 - SSC Modulation Deviation Test (HBR2CPAT)	350202	To evaluate the range of SSC down-spreading of the DUT's transmitted signal in ppm is within the conformance limits.
Lane 1 - SSC Modulation Deviation Test (Other Pattern)	359202	To evaluate the range of SSC down-spreading of the DUT's transmitted signal in ppm is within the conformance limits.
Lane 1 - SSC Modulation Deviation Test (PRBS 7)	351202	To evaluate the range of SSC down-spreading of the DUT's transmitted signal in ppm is within the conformance limits.
Lane 1 - SSC Modulation Deviation Test (PRBS 9)	352202	To evaluate the range of SSC down-spreading of the DUT's transmitted signal in ppm is within the conformance limits.
Lane 1 - SSC Modulation Deviation Test (Random Pattern)	358202	To evaluate the range of SSC down-spreading of the DUT's transmitted signal in ppm is within the conformance limits.
Lane 1 - SSC Modulation Frequency Test (D10.2)	303202	To evaluate the frequency of the SSC modulation and to validate it falls with specification limits.
Lane 1 - SSC Modulation Frequency Test (HBR2CPAT)	300202	To evaluate the frequency of the SSC modulation and to validate it falls with specification limits.
Lane 1 - SSC Modulation Frequency Test (Other Pattern)	309202	To evaluate the frequency of the SSC modulation and to validate it falls with specification limits.
Lane 1 - SSC Modulation Frequency Test (PRBS 7)	301202	To evaluate the frequency of the SSC modulation and to validate it falls with specification limits.
Lane 1 - SSC Modulation Frequency Test (PRBS 9)	302202	To evaluate the frequency of the SSC modulation and to validate it falls with specification limits.
Lane 1 - SSC Modulation Frequency Test (Random Pattern)	308202	To evaluate the frequency of the SSC modulation and to validate it falls with specification limits.



**Table 4** Test IDs and Names (continued)

Name	TestID	Description
Lane 1 - Total Jitter Test (TP3_EQ) (D10.2)	33202	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 1 - Total Jitter Test (TP3_EQ) (HBR2CPAT)	30202	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 1 - Total Jitter Test (TP3_EQ) (Other Pattern)	39202	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 1 - Total Jitter Test (TP3_EQ) (PRBS 7)	31202	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 1 - Total Jitter Test (TP3_EQ) (PRBS 9)	32202	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 1 - Total Jitter Test (TP3_EQ) (Random Pattern)	38202	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 1 / Lane 2 - Inter Pair Skew Test (HBR2CPAT)	130204	To evaluate the skew, or time delay, between differential main link data lanes of the eDP interface.
Lane 1 / Lane 2 - Inter Pair Skew Test (Other Pattern)	139204	To evaluate the skew, or time delay, between differential main link data lanes of the eDP interface.
Lane 1 / Lane 2 - Inter Pair Skew Test (PRBS 7)	131204	To evaluate the skew, or time delay, between differential main link data lanes of the eDP interface.
Lane 1 / Lane 2 - Inter Pair Skew Test (PRBS 9)	132204	To evaluate the skew, or time delay, between differential main link data lanes of the eDP interface.
Lane 1 / Lane 2 - Inter Pair Skew Test (Random Pattern)	138204	To evaluate the skew, or time delay, between differential main link data lanes of the eDP interface.
Lane 1 / Lane 3 - Inter Pair Skew Test (HBR2CPAT)	130205	To evaluate the skew, or time delay, between differential main link data lanes of the eDP interface.

**Table 4** Test IDs and Names (continued)

Name	TestID	Description
Lane 1 / Lane 3 - Inter Pair Skew Test (Other Pattern)	139205	To evaluate the skew, or time delay, between differential main link data lanes of the eDP interface.
Lane 1 / Lane 3 - Inter Pair Skew Test (PRBS 7)	131205	To evaluate the skew, or time delay, between differential main link data lanes of the eDP interface.
Lane 1 / Lane 3 - Inter Pair Skew Test (PRBS 9)	132205	To evaluate the skew, or time delay, between differential main link data lanes of the eDP interface.
Lane 1 / Lane 3 - Inter Pair Skew Test (Random Pattern)	138205	To evaluate the skew, or time delay, between differential main link data lanes of the eDP interface.
Lane 2 - AC Common Mode Noise Test (HBR2CPAT)	510203	To report common mode noise (unfiltered RMS) of the differential pairs of the eDP interface. These measurements can be useful in predicting the channels EMI/RFI performance.
Lane 2 - Deterministic Jitter Test (TP3_EQ) (D10.2)	43203	To evaluate the Deterministic Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 2 - Deterministic Jitter Test (TP3_EQ) (HBR2CPAT)	40203	To evaluate the Deterministic Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 2 - Deterministic Jitter Test (TP3_EQ) (Other Pattern)	49203	To evaluate the Deterministic Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 2 - Deterministic Jitter Test (TP3_EQ) (PRBS 7)	41203	To evaluate the Deterministic Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 2 - Deterministic Jitter Test (TP3_EQ) (PRBS 9)	42203	To evaluate the Deterministic Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 2 - Deterministic Jitter Test (TP3_EQ) (Random Pattern)	48203	To evaluate the Deterministic Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.

**Table 4** Test IDs and Names (continued)

Name	TestID	Description
Lane 2 - Differential Voltage Level Test (HBR2CPAT)	70203	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 2 - Differential Voltage Level Test (HBR2CPAT)	80203	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 2 - Differential Voltage Level Test (Other Pattern)	79203	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 2 - Differential Voltage Level Test (Other Pattern)	89203	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 2 - Differential Voltage Level Test (PLTPAT)	74203	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 2 - Differential Voltage Level Test (PLTPAT)	84203	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 2 - Differential Voltage Level Test (PRBS 7)	71203	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 2 - Differential Voltage Level Test (PRBS 7)	81203	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 2 - Differential Voltage Level Test (PRBS 9)	72203	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 2 - Differential Voltage Level Test (PRBS 9)	82203	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 2 - Differential Voltage Level Test (Random Pattern)	78203	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 2 - Differential Voltage Level Test (Random Pattern)	88203	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 2 - Eye Diagram Test (TP3_EQ) (D10.2)	13203	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
Lane 2 - Eye Diagram Test (TP3_EQ) (HBR2CPAT)	10203	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
Lane 2 - Eye Diagram Test (TP3_EQ) (Other Pattern)	19203	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.

**Table 4** Test IDs and Names (continued)

Name	TestID	Description
Lane 2 - Eye Diagram Test (TP3_EQ) (PRBS 7)	11203	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
Lane 2 - Eye Diagram Test (TP3_EQ) (PRBS 9)	12203	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
Lane 2 - Eye Diagram Test (TP3_EQ) (Random Pattern)	18203	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
Lane 2 - Fall Time Test (D10.2)	123203	To evaluate the differential fall time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 2 - Fall Time Test (HBR2CPAT)	120203	To evaluate the differential fall time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 2 - Fall Time Test (Other Pattern)	129203	To evaluate the differential fall time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 2 - Fall Time Test (PLTPAT)	124203	To evaluate the differential fall time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 2 - Fall Time Test (PRBS 7)	121203	To evaluate the differential fall time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 2 - Fall Time Test (PRBS 9)	122203	To evaluate the differential fall time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 2 - Fall Time Test (Random Pattern)	128203	To evaluate the differential fall time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.

**Table 4** Test IDs and Names (continued)

Name	TestID	Description
Lane 2 - Intra Pair Skew Test (D10.2)	503203	To evaluate the skew, or time delay, between the n and p legs of the differential pairs of the eDP interface. These measurements can be useful in predicting the channels EMI/RFI performance.
Lane 2 - Intra Pair Skew Test (HBR2CPAT)	500203	To evaluate the skew, or time delay, between the n and p legs of the differential pairs of the eDP interface. These measurements can be useful in predicting the channels EMI/RFI performance.
Lane 2 - Main Link Frequency Compliance Test (D10.2)	203203	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 2 - Main Link Frequency Compliance Test (D10.2)	253203	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 2 - Main Link Frequency Compliance Test (HBR2CPAT)	200203	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 2 - Main Link Frequency Compliance Test (HBR2CPAT)	250203	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 2 - Main Link Frequency Compliance Test (Other Pattern)	209203	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 2 - Main Link Frequency Compliance Test (Other Pattern)	259203	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 2 - Main Link Frequency Compliance Test (PRBS 7)	201203	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 2 - Main Link Frequency Compliance Test (PRBS 7)	251203	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 2 - Main Link Frequency Compliance Test (PRBS 9)	202203	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 2 - Main Link Frequency Compliance Test (PRBS 9)	252203	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 2 - Main Link Frequency Compliance Test (Random Pattern)	208203	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.

**Table 4** Test IDs and Names (continued)

Name	TestID	Description
Lane 2 - Main Link Frequency Compliance Test (Random Pattern)	258203	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 2 - Non ISI Jitter Test (D10.2)	23203	To evaluate the amount of eDP Non ISI jitter accompanying the data transmission.
Lane 2 - Non ISI Jitter Test (HBR2CPAT)	20203	To evaluate the amount of eDP Non ISI jitter accompanying the data transmission.
Lane 2 - Non ISI Jitter Test (Other Pattern)	29203	To evaluate the amount of eDP Non ISI jitter accompanying the data transmission.
Lane 2 - Non ISI Jitter Test (PRBS 7)	21203	To evaluate the amount of eDP Non ISI jitter accompanying the data transmission.
Lane 2 - Non ISI Jitter Test (PRBS 9)	22203	To evaluate the amount of eDP Non ISI jitter accompanying the data transmission.
Lane 2 - Non ISI Jitter Test (Random Pattern)	28203	To evaluate the amount of eDP Non ISI jitter accompanying the data transmission.
Lane 2 - Peak to Peak Differential Voltage Test (HBR2CPAT)	60203	To evaluate the peak to peak differential voltage of the DUT's transmitted signal is within the conformance limits.
Lane 2 - Peak to Peak Differential Voltage Test (Other Pattern)	69203	To evaluate the peak to peak differential voltage of the DUT's transmitted signal is within the conformance limits.
Lane 2 - Peak to Peak Differential Voltage Test (PLTPAT)	64203	To evaluate the peak to peak differential voltage of the DUT's transmitted signal is within the conformance limits.
Lane 2 - Peak to Peak Differential Voltage Test (PRBS 7)	61203	To evaluate the peak to peak differential voltage of the DUT's transmitted signal is within the conformance limits.
Lane 2 - Peak to Peak Differential Voltage Test (PRBS 9)	62203	To evaluate the peak to peak differential voltage of the DUT's transmitted signal is within the conformance limits.
Lane 2 - Peak to Peak Differential Voltage Test (Random Pattern)	68203	To evaluate the peak to peak differential voltage of the DUT's transmitted signal is within the conformance limits.
Lane 2 - Pre-Emphasis Level Test (HBR2CPAT)	90203	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 2 - Pre-Emphasis Level Test (HBR2CPAT)	100203	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 2 - Pre-Emphasis Level Test (Other Pattern)	99203	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.

**Table 4** Test IDs and Names (continued)

Name	TestID	Description
Lane 2 - Pre-Emphasis Level Test (Other Pattern)	109203	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 2 - Pre-Emphasis Level Test (PLTPAT)	94203	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 2 - Pre-Emphasis Level Test (PLTPAT)	104203	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 2 - Pre-Emphasis Level Test (PRBS 7)	91203	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 2 - Pre-Emphasis Level Test (PRBS 7)	101203	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 2 - Pre-Emphasis Level Test (PRBS 9)	92203	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 2 - Pre-Emphasis Level Test (PRBS 9)	102203	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 2 - Pre-Emphasis Level Test (Random Pattern)	98203	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 2 - Pre-Emphasis Level Test (Random Pattern)	108203	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 2 - Random Jitter Test (TP3_EQ) (D10.2)	53203	To evaluate the Random Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 2 - Random Jitter Test (TP3_EQ) (HBR2CPAT)	50203	To evaluate the Random Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 2 - Random Jitter Test (TP3_EQ) (Other Pattern)	59203	To evaluate the Random Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 2 - Random Jitter Test (TP3_EQ) (PRBS 7)	51203	To evaluate the Random Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.

**Table 4** Test IDs and Names (continued)

Name	TestID	Description
Lane 2 - Random Jitter Test (TP3_EQ) (PRBS 9)	52203	To evaluate the Random Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 2 - Random Jitter Test (TP3_EQ) (Random Pattern)	58203	To evaluate the Random Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 2 - Rise Time Test (D10.2)	113203	To evaluate the differential rise time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 2 - Rise Time Test (HBR2CPAT)	110203	To evaluate the differential rise time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 2 - Rise Time Test (Other Pattern)	119203	To evaluate the differential rise time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 2 - Rise Time Test (PLTPAT)	114203	To evaluate the differential rise time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 2 - Rise Time Test (PRBS 7)	111203	To evaluate the differential rise time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 2 - Rise Time Test (PRBS 9)	112203	To evaluate the differential rise time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 2 - Rise Time Test (Random Pattern)	118203	To evaluate the differential rise time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 2 - SSC Modulation Deviation Test (D10.2)	353203	To evaluate the range of SSC down-spreading of the DUT's transmitted signal in ppm is within the conformance limits.



**Table 4** Test IDs and Names (continued)

Name	TestID	Description
Lane 2 - SSC Modulation Deviation Test (HBR2CPAT)	350203	To evaluate the range of SSC down-spreading of the DUT's transmitted signal in ppm is within the conformance limits.
Lane 2 - SSC Modulation Deviation Test (Other Pattern)	359203	To evaluate the range of SSC down-spreading of the DUT's transmitted signal in ppm is within the conformance limits.
Lane 2 - SSC Modulation Deviation Test (PRBS 7)	351203	To evaluate the range of SSC down-spreading of the DUT's transmitted signal in ppm is within the conformance limits.
Lane 2 - SSC Modulation Deviation Test (PRBS 9)	352203	To evaluate the range of SSC down-spreading of the DUT's transmitted signal in ppm is within the conformance limits.
Lane 2 - SSC Modulation Deviation Test (Random Pattern)	358203	To evaluate the range of SSC down-spreading of the DUT's transmitted signal in ppm is within the conformance limits.
Lane 2 - SSC Modulation Frequency Test (D10.2)	303203	To evaluate the frequency of the SSC modulation and to validate it falls with specification limits.
Lane 2 - SSC Modulation Frequency Test (HBR2CPAT)	300203	To evaluate the frequency of the SSC modulation and to validate it falls with specification limits.
Lane 2 - SSC Modulation Frequency Test (Other Pattern)	309203	To evaluate the frequency of the SSC modulation and to validate it falls with specification limits.
Lane 2 - SSC Modulation Frequency Test (PRBS 7)	301203	To evaluate the frequency of the SSC modulation and to validate it falls with specification limits.
Lane 2 - SSC Modulation Frequency Test (PRBS 9)	302203	To evaluate the frequency of the SSC modulation and to validate it falls with specification limits.
Lane 2 - SSC Modulation Frequency Test (Random Pattern)	308203	To evaluate the frequency of the SSC modulation and to validate it falls with specification limits.
Lane 2 - Total Jitter Test (TP3_EQ) (D10.2)	33203	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 2 - Total Jitter Test (TP3_EQ) (HBR2CPAT)	30203	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.

**Table 4** Test IDs and Names (continued)

Name	TestID	Description
Lane 2 - Total Jitter Test (TP3_EQ) (Other Pattern)	39203	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 2 - Total Jitter Test (TP3_EQ) (PRBS 7)	31203	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 2 - Total Jitter Test (TP3_EQ) (PRBS 9)	32203	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 2 - Total Jitter Test (TP3_EQ) (Random Pattern)	38203	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 2 / Lane 3 - Inter Pair Skew Test (HBR2CPAT)	130206	To evaluate the skew, or time delay, between differential main link data lanes of the eDP interface.
Lane 2 / Lane 3 - Inter Pair Skew Test (Other Pattern)	139206	To evaluate the skew, or time delay, between differential main link data lanes of the eDP interface.
Lane 2 / Lane 3 - Inter Pair Skew Test (PRBS 7)	131206	To evaluate the skew, or time delay, between differential main link data lanes of the eDP interface.
Lane 2 / Lane 3 - Inter Pair Skew Test (PRBS 9)	132206	To evaluate the skew, or time delay, between differential main link data lanes of the eDP interface.
Lane 2 / Lane 3 - Inter Pair Skew Test (Random Pattern)	138206	To evaluate the skew, or time delay, between differential main link data lanes of the eDP interface.
Lane 3 - AC Common Mode Noise Test (HBR2CPAT)	510204	To report common mode noise (unfiltered RMS) of the differential pairs of the eDP interface. These measurements can be useful in predicting the channels EMI/RFI performance.
Lane 3 - Deterministic Jitter Test (TP3_EQ) (D10.2)	43204	To evaluate the Deterministic Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.

**Table 4** Test IDs and Names (continued)

Name	TestID	Description
Lane 3 - Deterministic Jitter Test (TP3_EQ) (HBR2CPAT)	40204	To evaluate the Deterministic Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 3 - Deterministic Jitter Test (TP3_EQ) (Other Pattern)	49204	To evaluate the Deterministic Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 3 - Deterministic Jitter Test (TP3_EQ) (PRBS 7)	41204	To evaluate the Deterministic Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 3 - Deterministic Jitter Test (TP3_EQ) (PRBS 9)	42204	To evaluate the Deterministic Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 3 - Deterministic Jitter Test (TP3_EQ) (Random Pattern)	48204	To evaluate the Deterministic Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 3 - Differential Voltage Level Test (HBR2CPAT)	70204	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 3 - Differential Voltage Level Test (HBR2CPAT)	80204	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 3 - Differential Voltage Level Test (Other Pattern)	79204	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 3 - Differential Voltage Level Test (Other Pattern)	89204	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 3 - Differential Voltage Level Test (PLTPAT)	74204	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 3 - Differential Voltage Level Test (PLTPAT)	84204	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 3 - Differential Voltage Level Test (PRBS 7)	71204	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 3 - Differential Voltage Level Test (PRBS 7)	81204	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.

**Table 4** Test IDs and Names (continued)

Name	TestID	Description
Lane 3 - Differential Voltage Level Test (PRBS 9)	72204	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 3 - Differential Voltage Level Test (PRBS 9)	82204	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 3 - Differential Voltage Level Test (Random Pattern)	78204	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 3 - Differential Voltage Level Test (Random Pattern)	88204	To evaluate the differential voltage level of the DUT's transmitted signal is within the conformance limits.
Lane 3 - Eye Diagram Test (TP3_EQ) (D10.2)	13204	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
Lane 3 - Eye Diagram Test (TP3_EQ) (HBR2CPAT)	10204	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
Lane 3 - Eye Diagram Test (TP3_EQ) (Other Pattern)	19204	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
Lane 3 - Eye Diagram Test (TP3_EQ) (PRBS 7)	11204	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
Lane 3 - Eye Diagram Test (TP3_EQ) (PRBS 9)	12204	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
Lane 3 - Eye Diagram Test (TP3_EQ) (Random Pattern)	18204	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
Lane 3 - Fall Time Test (D10.2)	123204	To evaluate the differential fall time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 3 - Fall Time Test (HBR2CPAT)	120204	To evaluate the differential fall time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.

**Table 4** Test IDs and Names (continued)

Name	TestID	Description
Lane 3 - Fall Time Test (Other Pattern)	129204	To evaluate the differential fall time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 3 - Fall Time Test (PLTPAT)	124204	To evaluate the differential fall time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 3 - Fall Time Test (PRBS 7)	121204	To evaluate the differential fall time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 3 - Fall Time Test (PRBS 9)	122204	To evaluate the differential fall time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 3 - Fall Time Test (Random Pattern)	128204	To evaluate the differential fall time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 3 - Intra Pair Skew Test (D10.2)	503204	To evaluate the skew, or time delay, between the n and p legs of the differential pairs of the eDP interface. These measurements can be useful in predicting the channels EMI/RFI performance.
Lane 3 - Intra Pair Skew Test (HBR2CPAT)	500204	To evaluate the skew, or time delay, between the n and p legs of the differential pairs of the eDP interface. These measurements can be useful in predicting the channels EMI/RFI performance.
Lane 3 - Main Link Frequency Compliance Test (D10.2)	203204	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 3 - Main Link Frequency Compliance Test (D10.2)	253204	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 3 - Main Link Frequency Compliance Test (HBR2CPAT)	200204	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 3 - Main Link Frequency Compliance Test (HBR2CPAT)	250204	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.

**Table 4** Test IDs and Names (continued)

Name	TestID	Description
Lane 3 - Main Link Frequency Compliance Test (Other Pattern)	209204	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 3 - Main Link Frequency Compliance Test (Other Pattern)	259204	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 3 - Main Link Frequency Compliance Test (PRBS 7)	201204	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 3 - Main Link Frequency Compliance Test (PRBS 7)	251204	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 3 - Main Link Frequency Compliance Test (PRBS 9)	202204	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 3 - Main Link Frequency Compliance Test (PRBS 9)	252204	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 3 - Main Link Frequency Compliance Test (Random Pattern)	208204	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 3 - Main Link Frequency Compliance Test (Random Pattern)	258204	To evaluate the data rate variation of the DUT's transmitted signal under all conditions is within the conformance limits.
Lane 3 - Non ISI Jitter Test (D10.2)	23204	To evaluate the amount of eDP Non ISI jitter accompanying the data transmission.
Lane 3 - Non ISI Jitter Test (HBR2CPAT)	20204	To evaluate the amount of eDP Non ISI jitter accompanying the data transmission.
Lane 3 - Non ISI Jitter Test (Other Pattern)	29204	To evaluate the amount of eDP Non ISI jitter accompanying the data transmission.
Lane 3 - Non ISI Jitter Test (PRBS 7)	21204	To evaluate the amount of eDP Non ISI jitter accompanying the data transmission.
Lane 3 - Non ISI Jitter Test (PRBS 9)	22204	To evaluate the amount of eDP Non ISI jitter accompanying the data transmission.
Lane 3 - Non ISI Jitter Test (Random Pattern)	28204	To evaluate the amount of eDP Non ISI jitter accompanying the data transmission.
Lane 3 - Peak to Peak Differential Voltage Test (HBR2CPAT)	60204	To evaluate the peak to peak differential voltage of the DUT's transmitted signal is within the conformance limits.

**Table 4** Test IDs and Names (continued)

Name	TestID	Description
Lane 3 - Peak to Peak Differential Voltage Test (Other Pattern)	69204	To evaluate the peak to peak differential voltage of the DUT's transmitted signal is within the conformance limits.
Lane 3 - Peak to Peak Differential Voltage Test (PLTPAT)	64204	To evaluate the peak to peak differential voltage of the DUT's transmitted signal is within the conformance limits.
Lane 3 - Peak to Peak Differential Voltage Test (PRBS 7)	61204	To evaluate the peak to peak differential voltage of the DUT's transmitted signal is within the conformance limits.
Lane 3 - Peak to Peak Differential Voltage Test (PRBS 9)	62204	To evaluate the peak to peak differential voltage of the DUT's transmitted signal is within the conformance limits.
Lane 3 - Peak to Peak Differential Voltage Test (Random Pattern)	68204	To evaluate the peak to peak differential voltage of the DUT's transmitted signal is within the conformance limits.
Lane 3 - Pre-Emphasis Level Test (HBR2CPAT)	90204	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 3 - Pre-Emphasis Level Test (HBR2CPAT)	100204	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 3 - Pre-Emphasis Level Test (Other Pattern)	99204	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 3 - Pre-Emphasis Level Test (Other Pattern)	109204	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 3 - Pre-Emphasis Level Test (PLTPAT)	94204	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 3 - Pre-Emphasis Level Test (PLTPAT)	104204	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 3 - Pre-Emphasis Level Test (PRBS 7)	91204	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 3 - Pre-Emphasis Level Test (PRBS 7)	101204	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 3 - Pre-Emphasis Level Test (PRBS 9)	92204	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 3 - Pre-Emphasis Level Test (PRBS 9)	102204	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 3 - Pre-Emphasis Level Test (Random Pattern)	98204	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.
Lane 3 - Pre-Emphasis Level Test (Random Pattern)	108204	To evaluate the pre-emphasis level of the DUT's transmitted signal is within the conformance limits.

**Table 4** Test IDs and Names (continued)

Name	TestID	Description
Lane 3 - Random Jitter Test (TP3_EQ) (D10.2)	53204	To evaluate the Random Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 3 - Random Jitter Test (TP3_EQ) (HBR2CPAT)	50204	To evaluate the Random Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 3 - Random Jitter Test (TP3_EQ) (Other Pattern)	59204	To evaluate the Random Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 3 - Random Jitter Test (TP3_EQ) (PRBS 7)	51204	To evaluate the Random Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 3 - Random Jitter Test (TP3_EQ) (PRBS 9)	52204	To evaluate the Random Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 3 - Random Jitter Test (TP3_EQ) (Random Pattern)	58204	To evaluate the Random Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 3 - Rise Time Test (D10.2)	113204	To evaluate the differential rise time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 3 - Rise Time Test (HBR2CPAT)	110204	To evaluate the differential rise time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 3 - Rise Time Test (Other Pattern)	119204	To evaluate the differential rise time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.



**Table 4** Test IDs and Names (continued)

Name	TestID	Description
Lane 3 - Rise Time Test (PLTPAT)	114204	To evaluate the differential rise time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 3 - Rise Time Test (PRBS 7)	111204	To evaluate the differential rise time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 3 - Rise Time Test (PRBS 9)	112204	To evaluate the differential rise time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 3 - Rise Time Test (Random Pattern)	118204	To evaluate the differential rise time of the main link data lanes of the eDP interface. These measurement can be useful in predicting the channels EMI/RFI performance.
Lane 3 - SSC Modulation Deviation Test (D10.2)	353204	To evaluate the range of SSC down-spreading of the DUT's transmitted signal in ppm is within the conformance limits.
Lane 3 - SSC Modulation Deviation Test (HBR2CPAT)	350204	To evaluate the range of SSC down-spreading of the DUT's transmitted signal in ppm is within the conformance limits.
Lane 3 - SSC Modulation Deviation Test (Other Pattern)	359204	To evaluate the range of SSC down-spreading of the DUT's transmitted signal in ppm is within the conformance limits.
Lane 3 - SSC Modulation Deviation Test (PRBS 7)	351204	To evaluate the range of SSC down-spreading of the DUT's transmitted signal in ppm is within the conformance limits.
Lane 3 - SSC Modulation Deviation Test (PRBS 9)	352204	To evaluate the range of SSC down-spreading of the DUT's transmitted signal in ppm is within the conformance limits.
Lane 3 - SSC Modulation Deviation Test (Random Pattern)	358204	To evaluate the range of SSC down-spreading of the DUT's transmitted signal in ppm is within the conformance limits.
Lane 3 - SSC Modulation Frequency Test (D10.2)	303204	To evaluate the frequency of the SSC modulation and to validate it falls with specification limits.
Lane 3 - SSC Modulation Frequency Test (HBR2CPAT)	300204	To evaluate the frequency of the SSC modulation and to validate it falls with specification limits.
Lane 3 - SSC Modulation Frequency Test (Other Pattern)	309204	To evaluate the frequency of the SSC modulation and to validate it falls with specification limits.

**Table 4** Test IDs and Names (continued)

Name	TestID	Description
Lane 3 - SSC Modulation Frequency Test (PRBS 7)	301204	To evaluate the frequency of the SSC modulation and to validate it falls with specification limits.
Lane 3 - SSC Modulation Frequency Test (PRBS 9)	302204	To evaluate the frequency of the SSC modulation and to validate it falls with specification limits.
Lane 3 - SSC Modulation Frequency Test (Random Pattern)	308204	To evaluate the frequency of the SSC modulation and to validate it falls with specification limits.
Lane 3 - Total Jitter Test (TP3_EQ) (D10.2)	33204	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 3 - Total Jitter Test (TP3_EQ) (HBR2CPAT)	30204	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 3 - Total Jitter Test (TP3_EQ) (Other Pattern)	39204	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 3 - Total Jitter Test (TP3_EQ) (PRBS 7)	31204	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 3 - Total Jitter Test (TP3_EQ) (PRBS 9)	32204	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 3 - Total Jitter Test (TP3_EQ) (Random Pattern)	38204	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Offline Capture Waveform	101	To capture all waveforms required for compliance testing.
eDP Equalizer Settings	108	

## 4 Instruments

The following table shows the instruments used by this application. The name is required by various remote interface methods.

- Instrument Name – The name to use as a parameter in remote interface commands.
- Description – The description of the instrument.

For example, if an application uses an oscilloscope and a pulse generator, then you would expect to see something like this in the table below:

**Table 5** Example Instrument Information

Name	Description
scope	The primary oscilloscope.
Pulse	The pulse generator used for Gen 2 tests.

and you would be able to remotely control an instrument using:

ARSL syntax (replace [description] with actual parameter)

```
-----  
arsl -a ipaddress -c "SendScpiCommandCustom 'Command=[scpi  
command];Timeout=100;Instrument=pulsegen'"
```

```
arsl -a ipaddress -c "SendScpiQueryCustom 'Command=[scpi  
query];Timeout=100;Instrument=pulsegen'"
```

C# syntax (replace [description] with actual parameter)

```
-----  
SendScpiCommandOptions commandOptions = new SendScpiCommandOptions();  
commandOptions.Command = "[scpi command]";  
commandOptions.Instrument = "[instrument name]";  
commandOptions.Timeout = [timeout];  
remoteAte.SendScpiCommand(commandOptions);
```

```
SendScpiQueryOptions queryOptions = new SendScpiQueryOptions();  
queryOptions.Query = "[scpi query]";  
queryOptions.Instrument = "[instrument name]";
```

```
queryOptions.Timeout = [timeout];  
remoteAte.SendScpiQuery(queryOptions);
```

Here are the actual instrument names used by this application:

**NOTE**

The file, "InstrumentInfo.txt", which may be found in the same directory as this help file, contains all of the information found in the table below in a format suitable for parsing.

---

**Table 6** Instrument Names

Instrument Name	Description
scope	The primary oscilloscope

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